

FIG. 1a

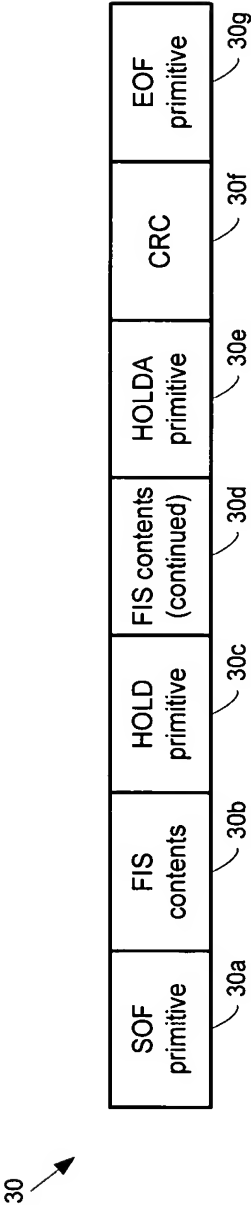


FIG. 1b

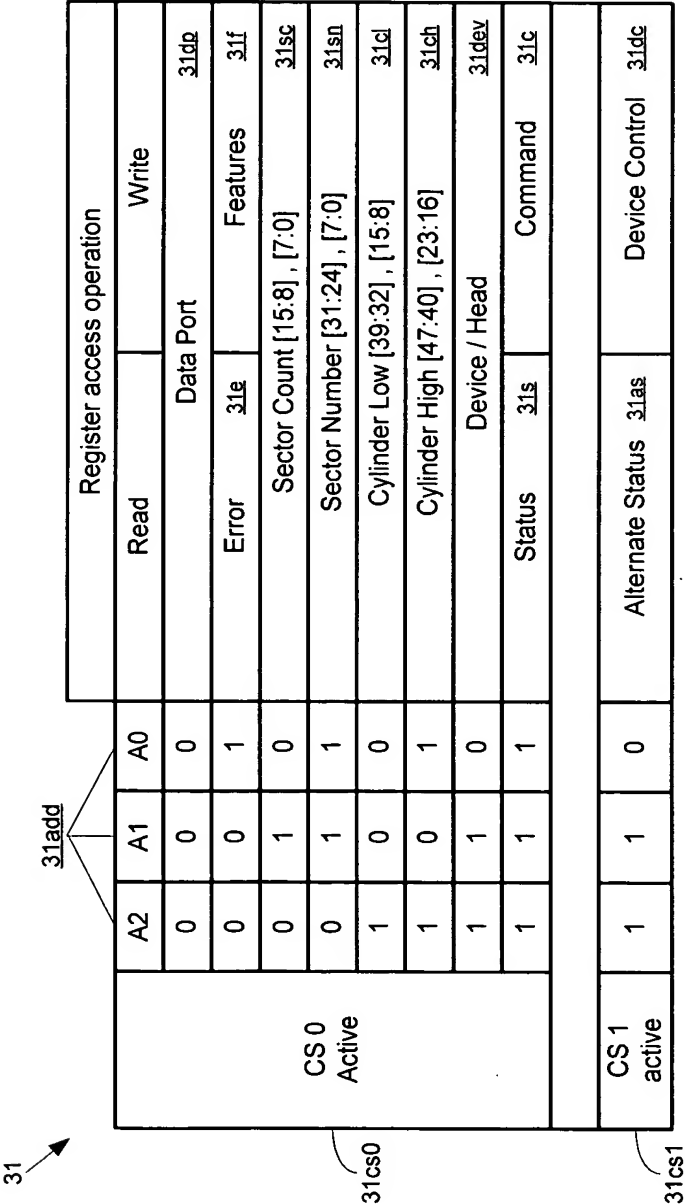


FIG. 1c

0	Features	Command	C	R	R	Reserved (0)	FIS Type (27h)
1	Dev / Head	Cyl High	Cyl Low				Sector Number
2	Features (exp)	Cyl High (exp)	Cyl Low (exp)				Sector Num (exp)
3	Control	Reserved (0)	Sector Count (exp)				Sector Count
4	Reserved (0)	Reserved (0)	Reserved (0)				Reserved (0)

FIG. 1d(i) Register FIS Host to Device

[illegible]

FIG. 1d(iii) DMA Activate FIS, Device to Host

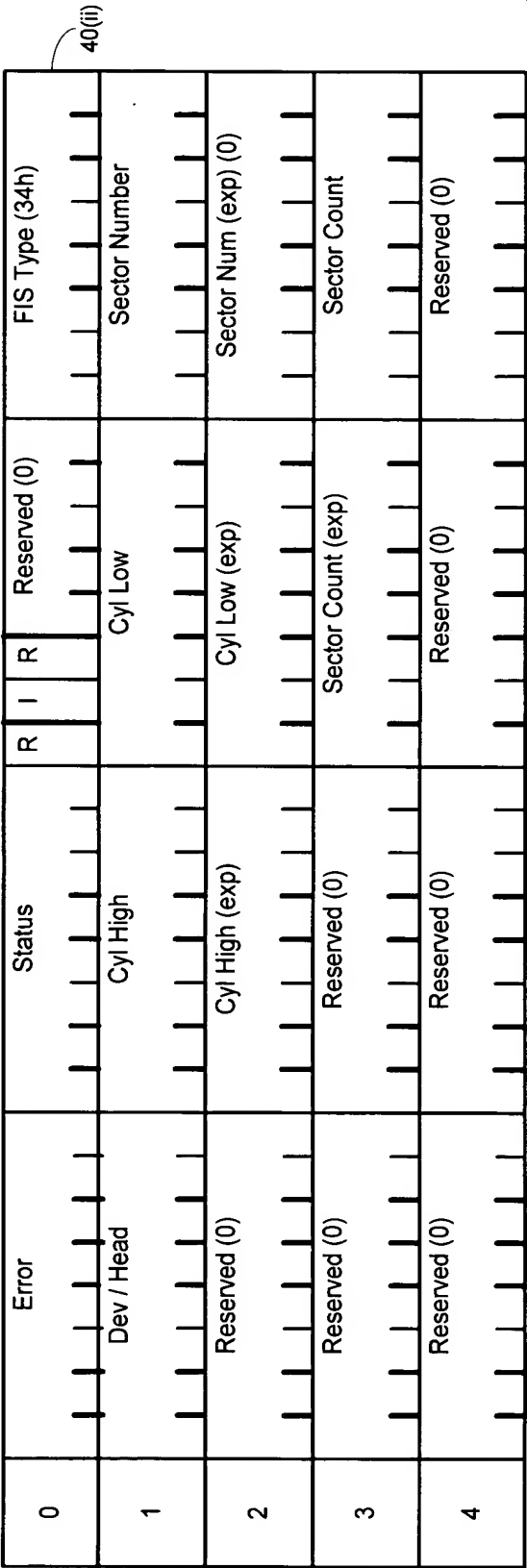


FIG. 1d(ii) Register FIS Device to Host

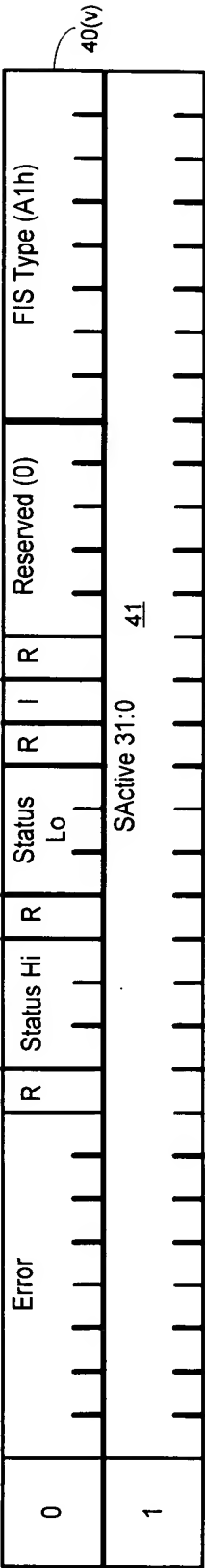


FIG. 1d(v) Set Device Bits FIS

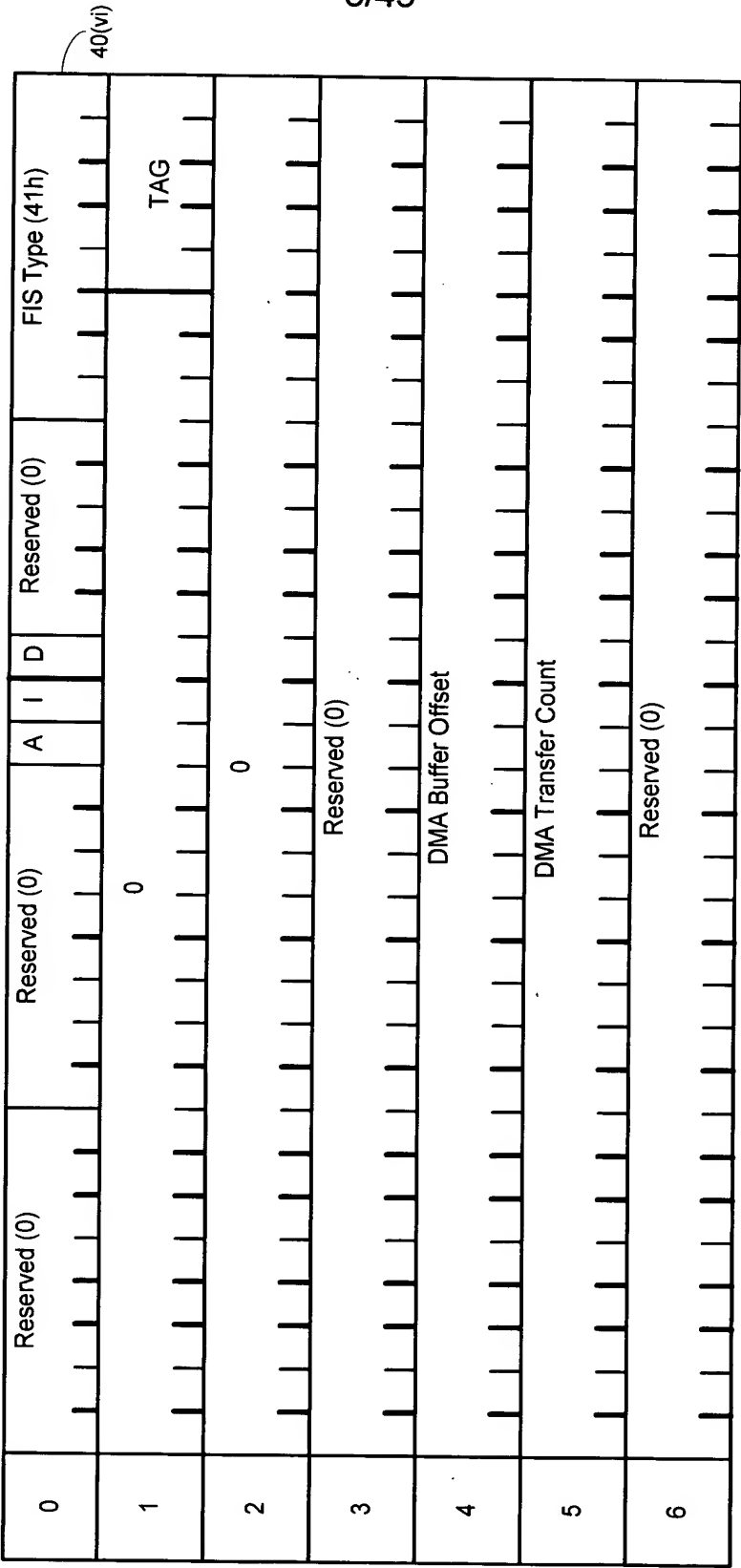


FIG. 1d(iv) DMA Setup FIS

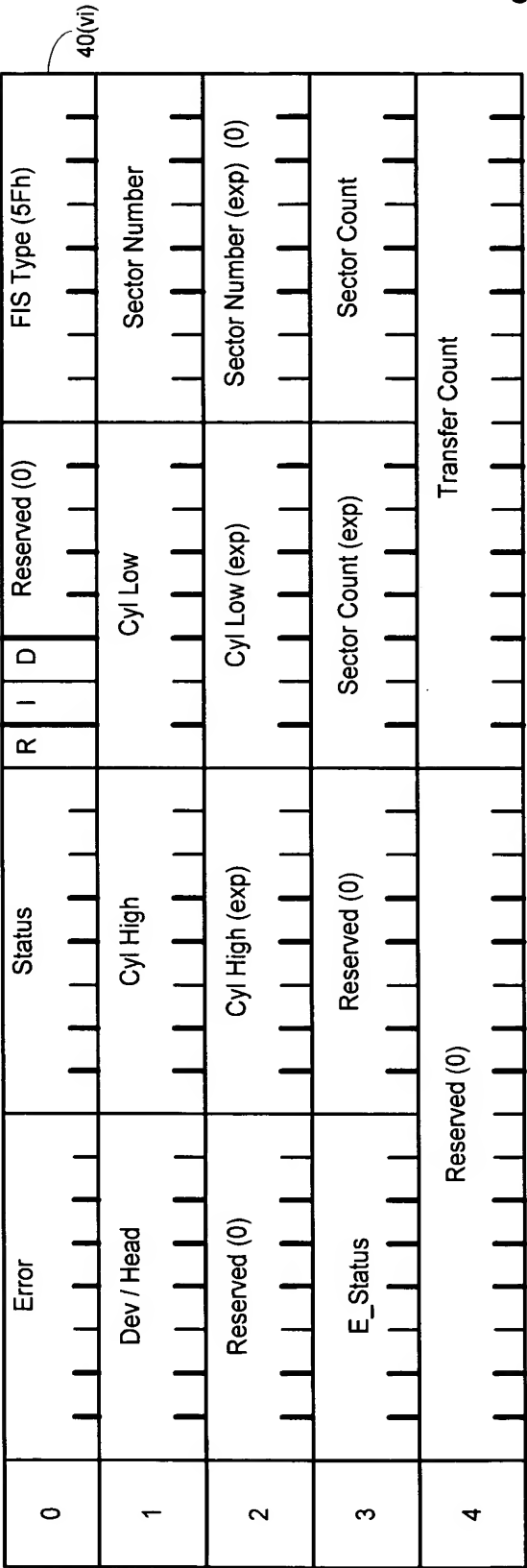


FIG. 1d(vi) PIO Setup FIS

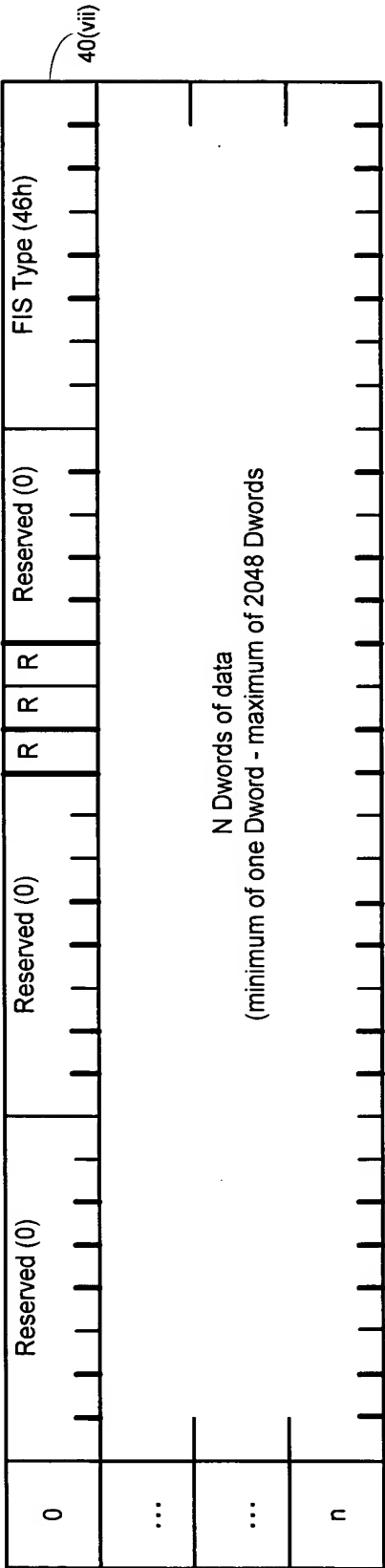


FIG. 1d(vii) Data FIS

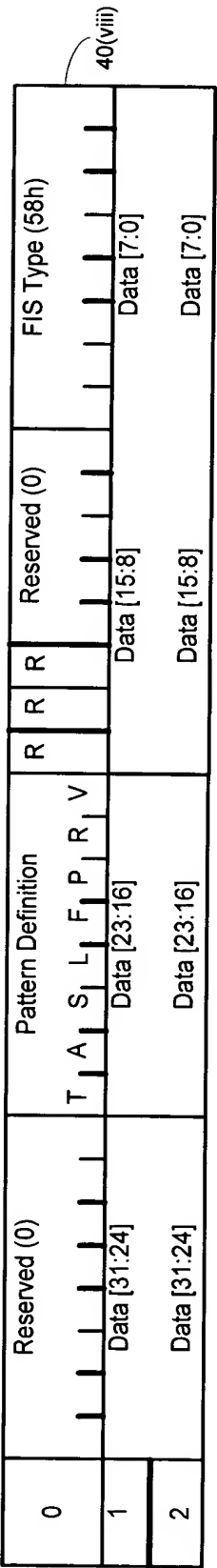


FIG. 1d (viii) BIST Activate FIS

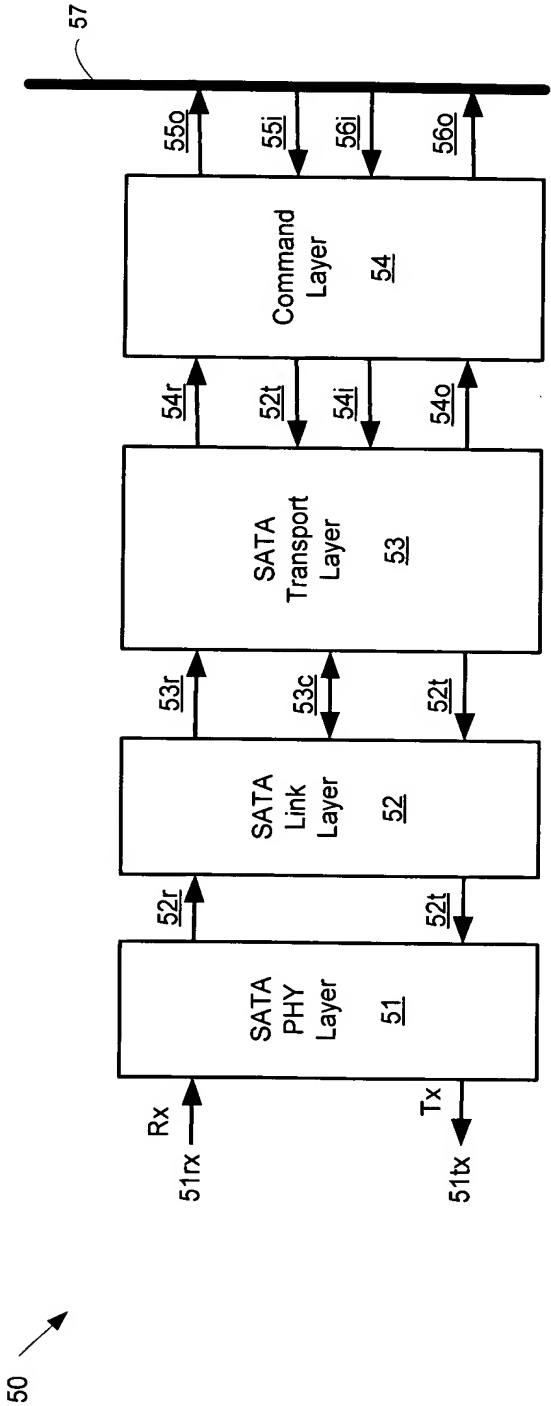


FIG. 2a

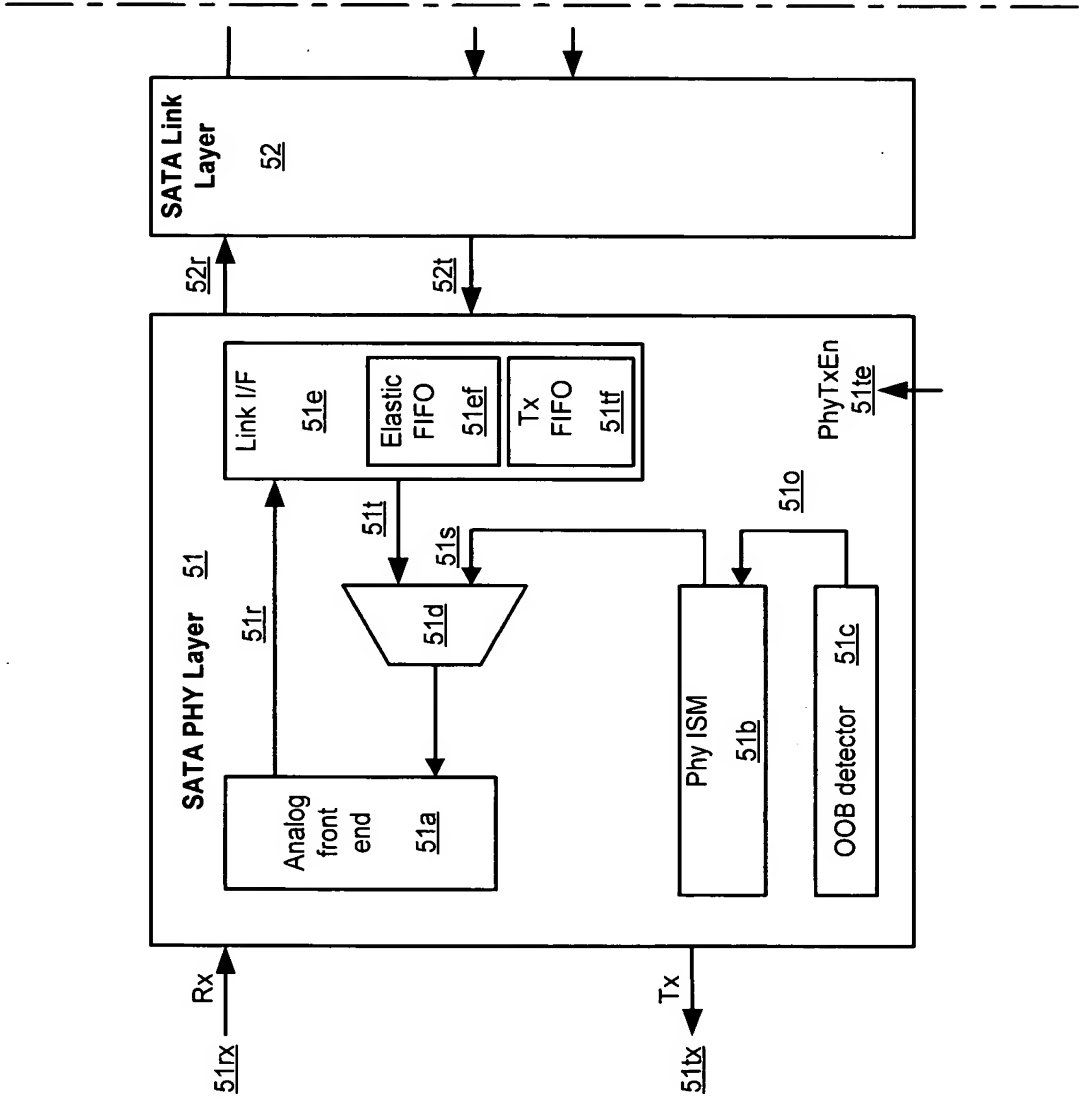


FIG. 2b(i)

Fig. 2b(i)	Fig. 2b(ii)
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Key To
FIG. 2b

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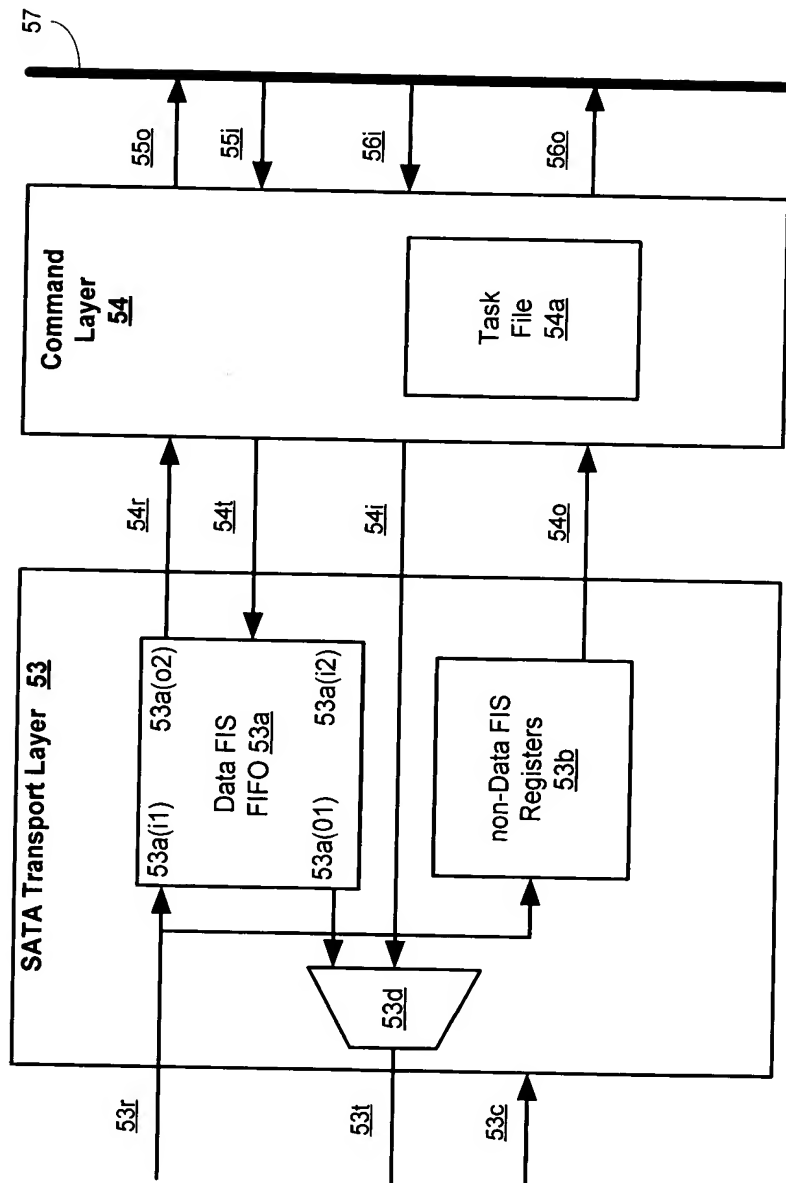


FIG. 2b(ii)

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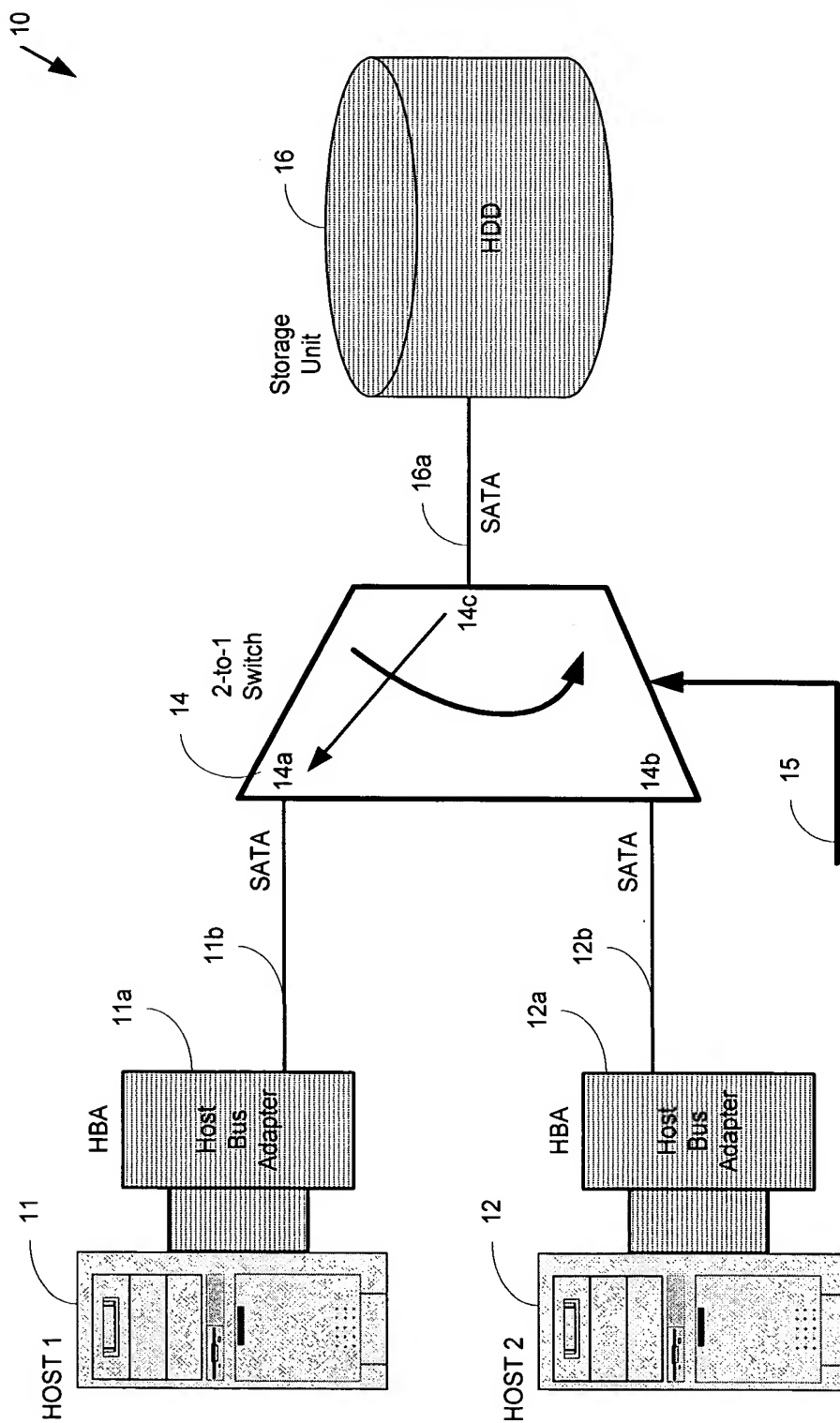


FIG. 3a

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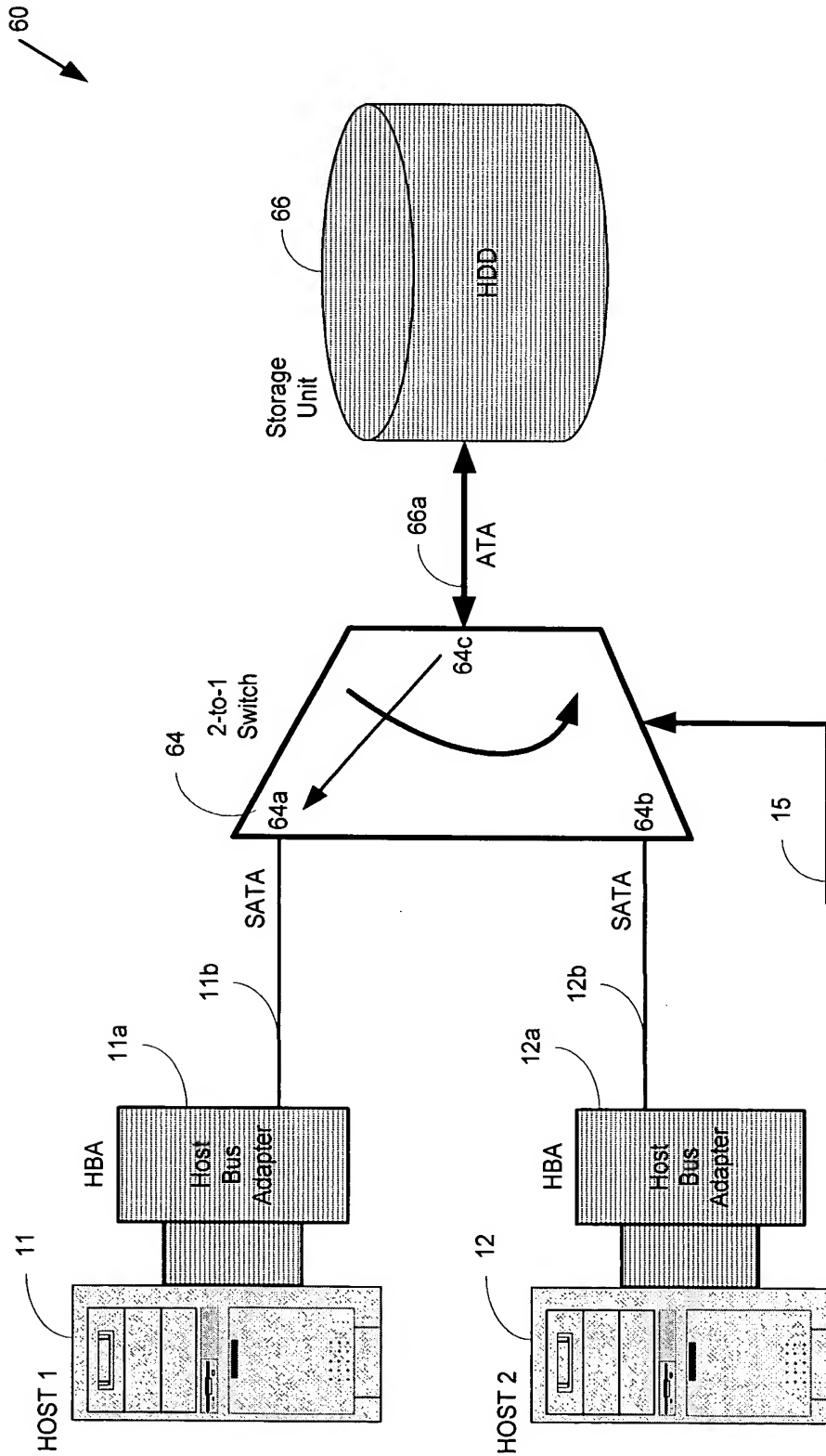


FIG. 3b



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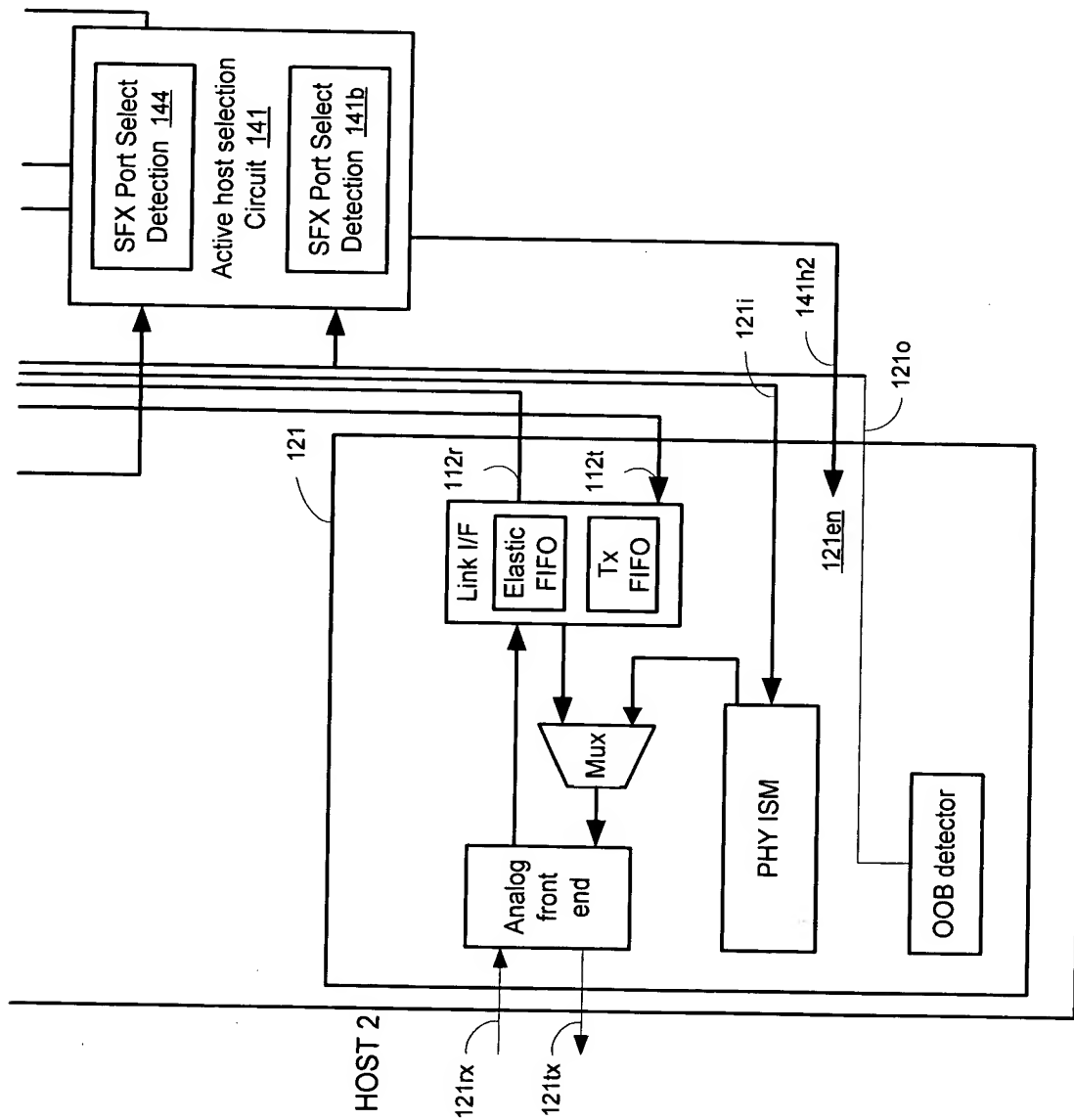


FIG. 4b

FIG. 5a	FIG. 5b
FIG. 5c	Key To FIG. 5

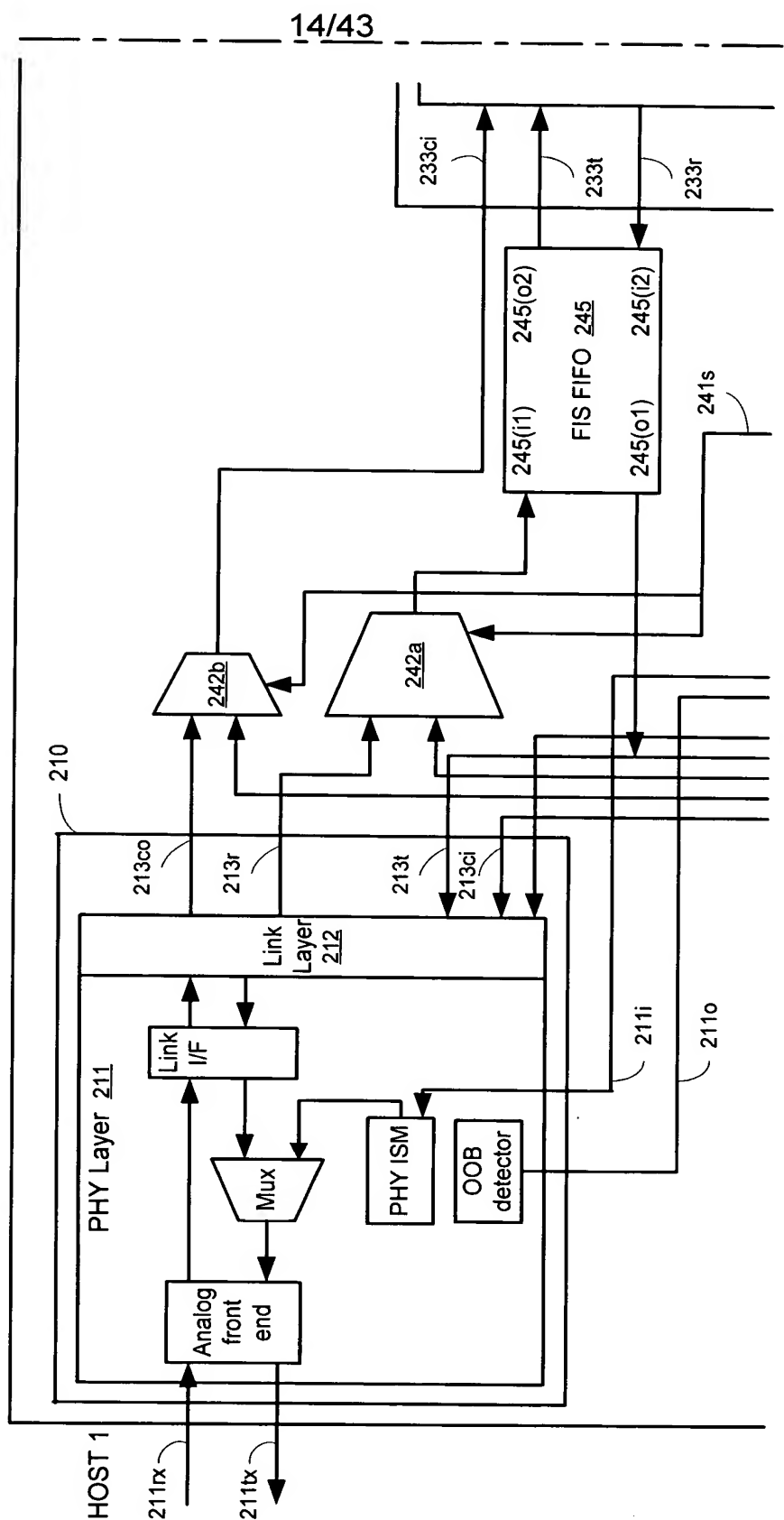
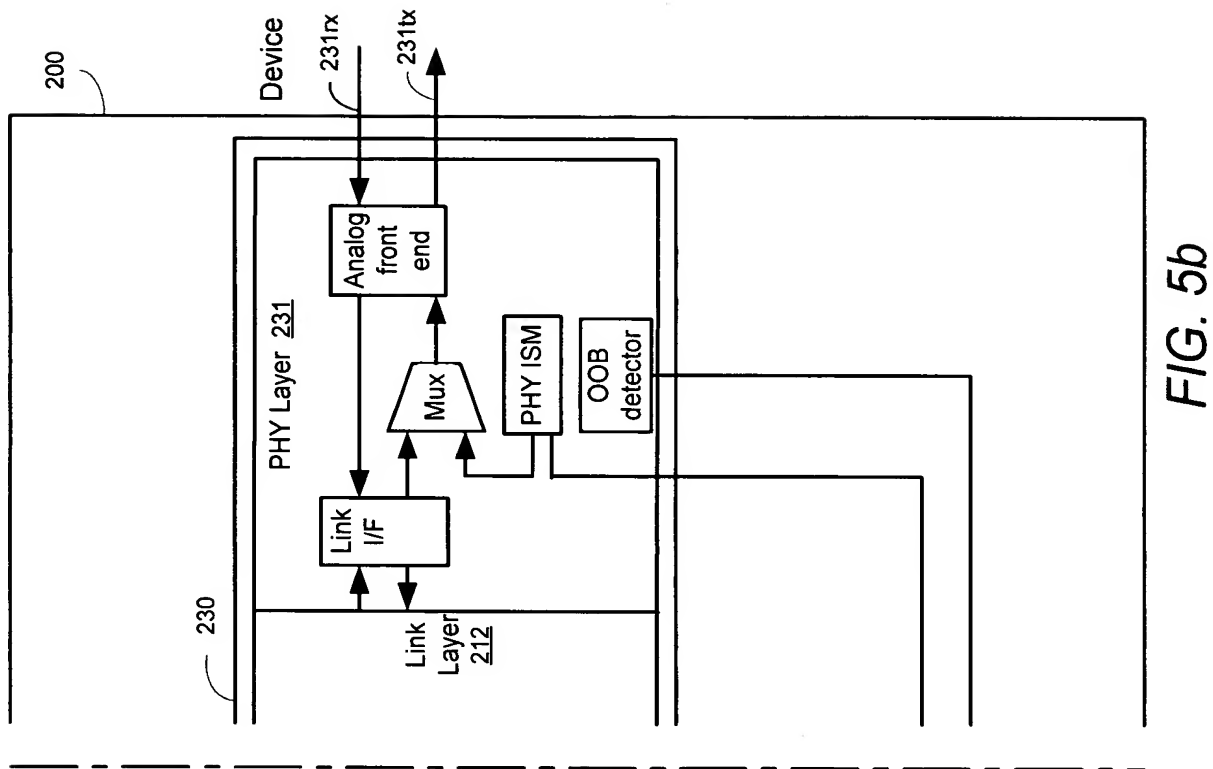


FIG. 5a



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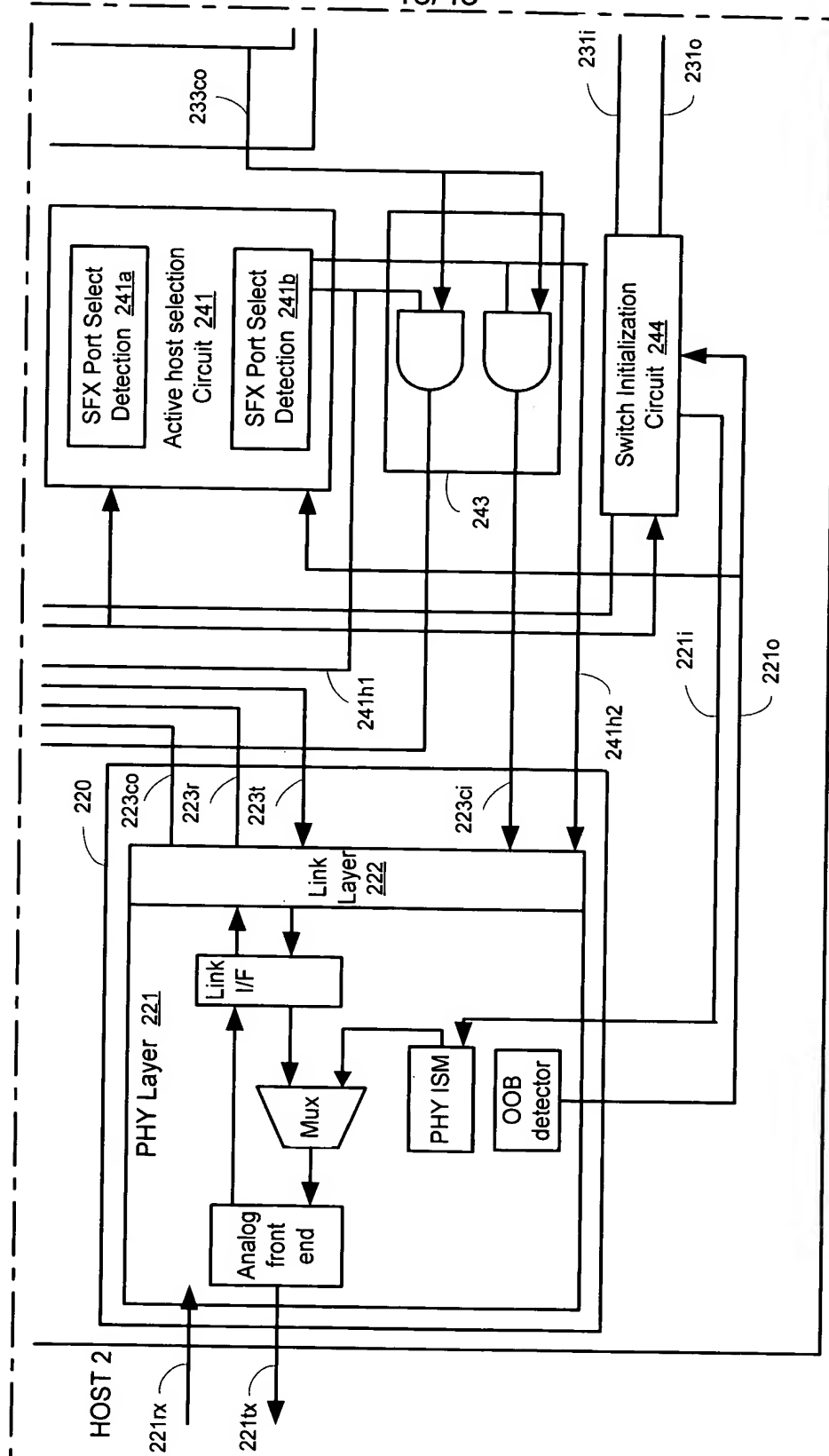


FIG. 5c

FIG. 6a FIG. 6b

Key To
 FIG. 6

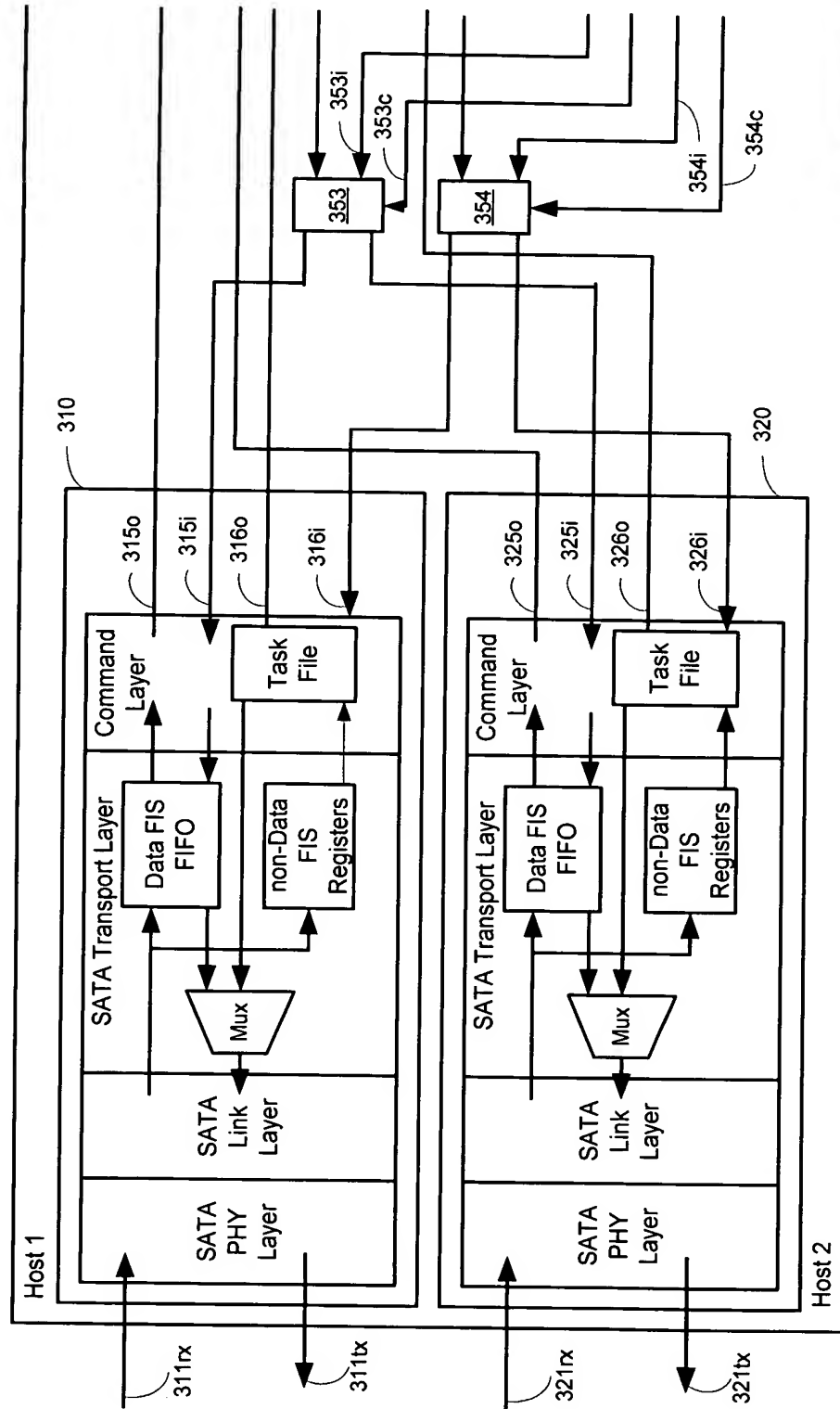


FIG. 6a

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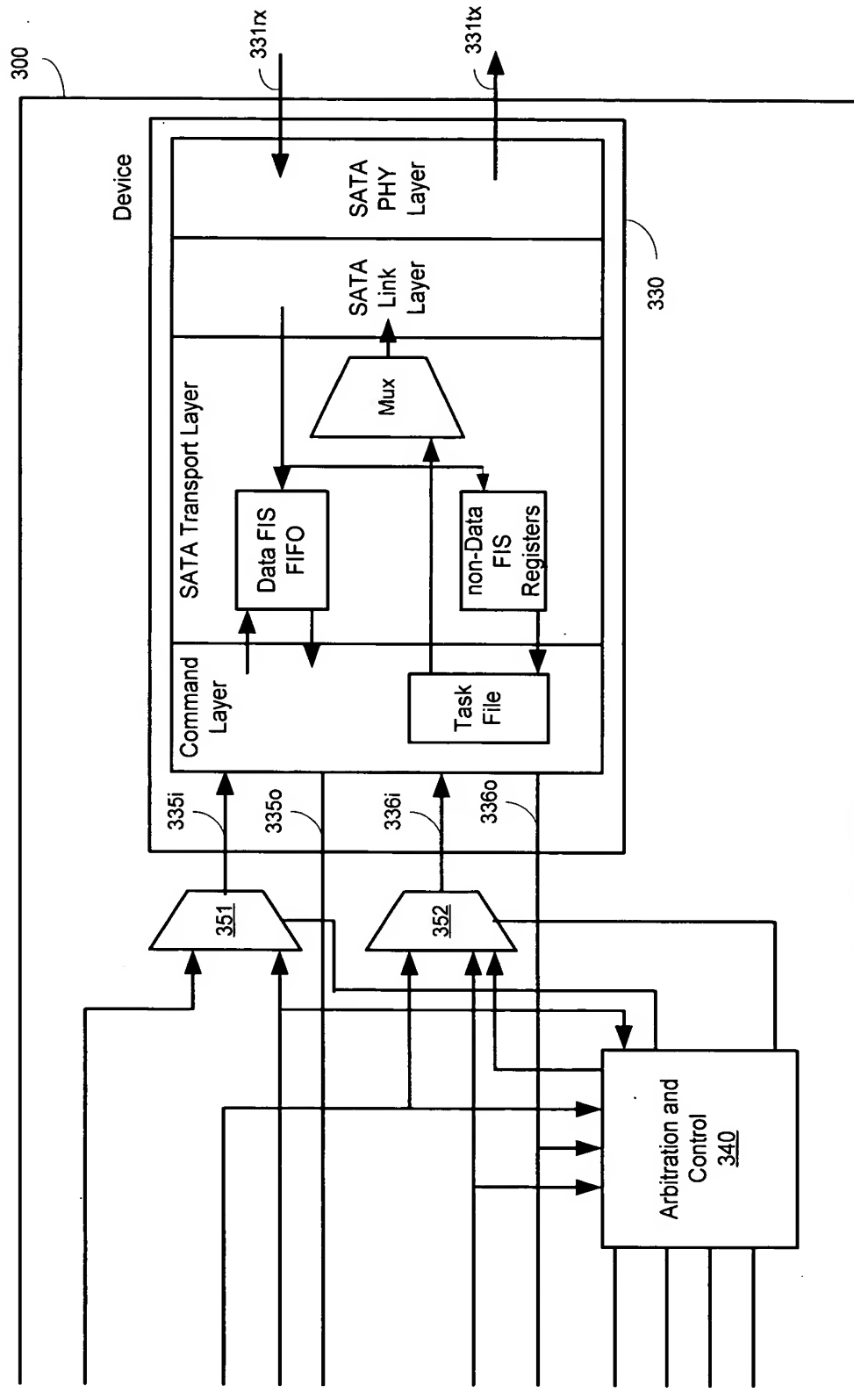


FIG. 6b

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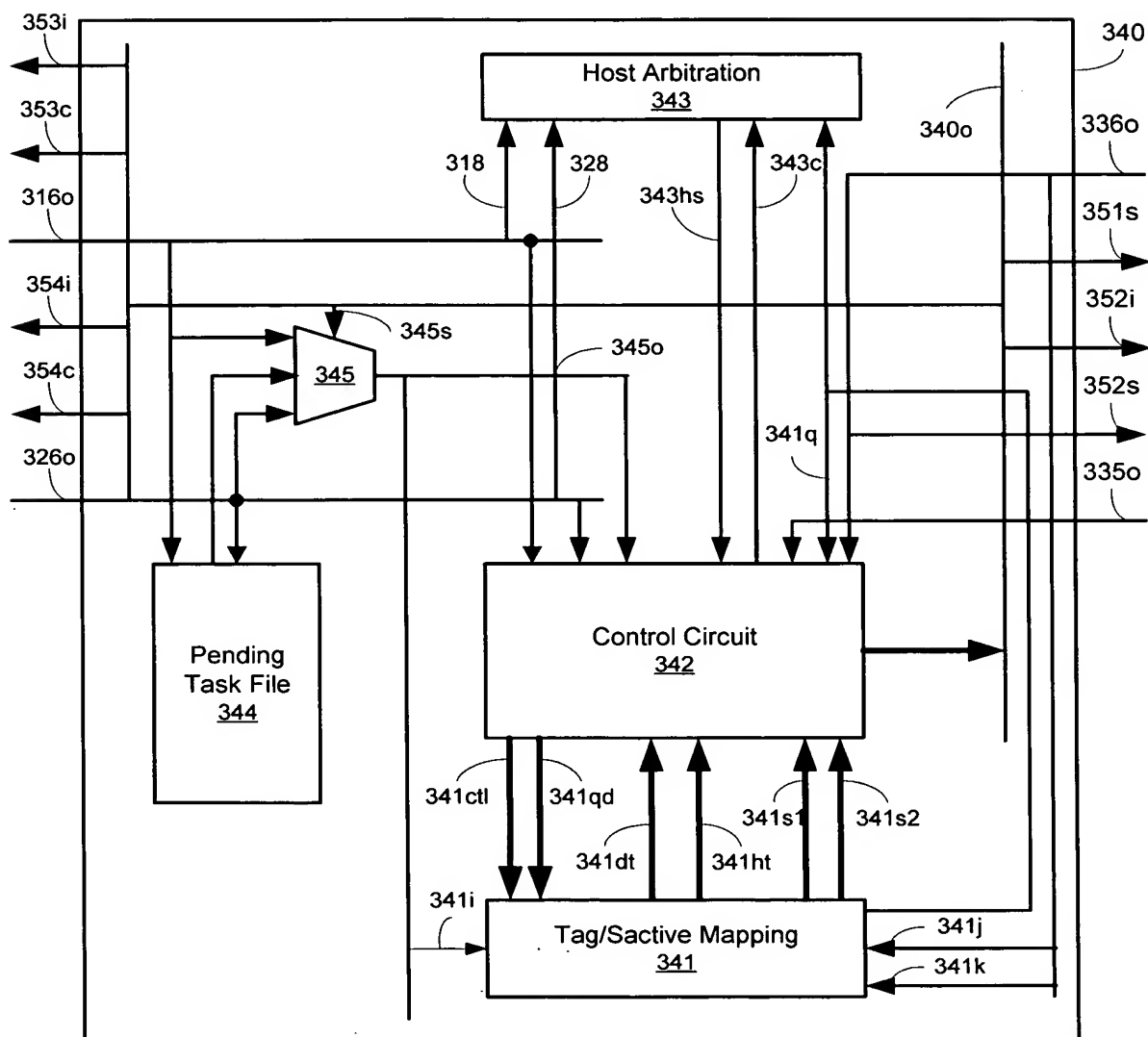


FIG. 7a

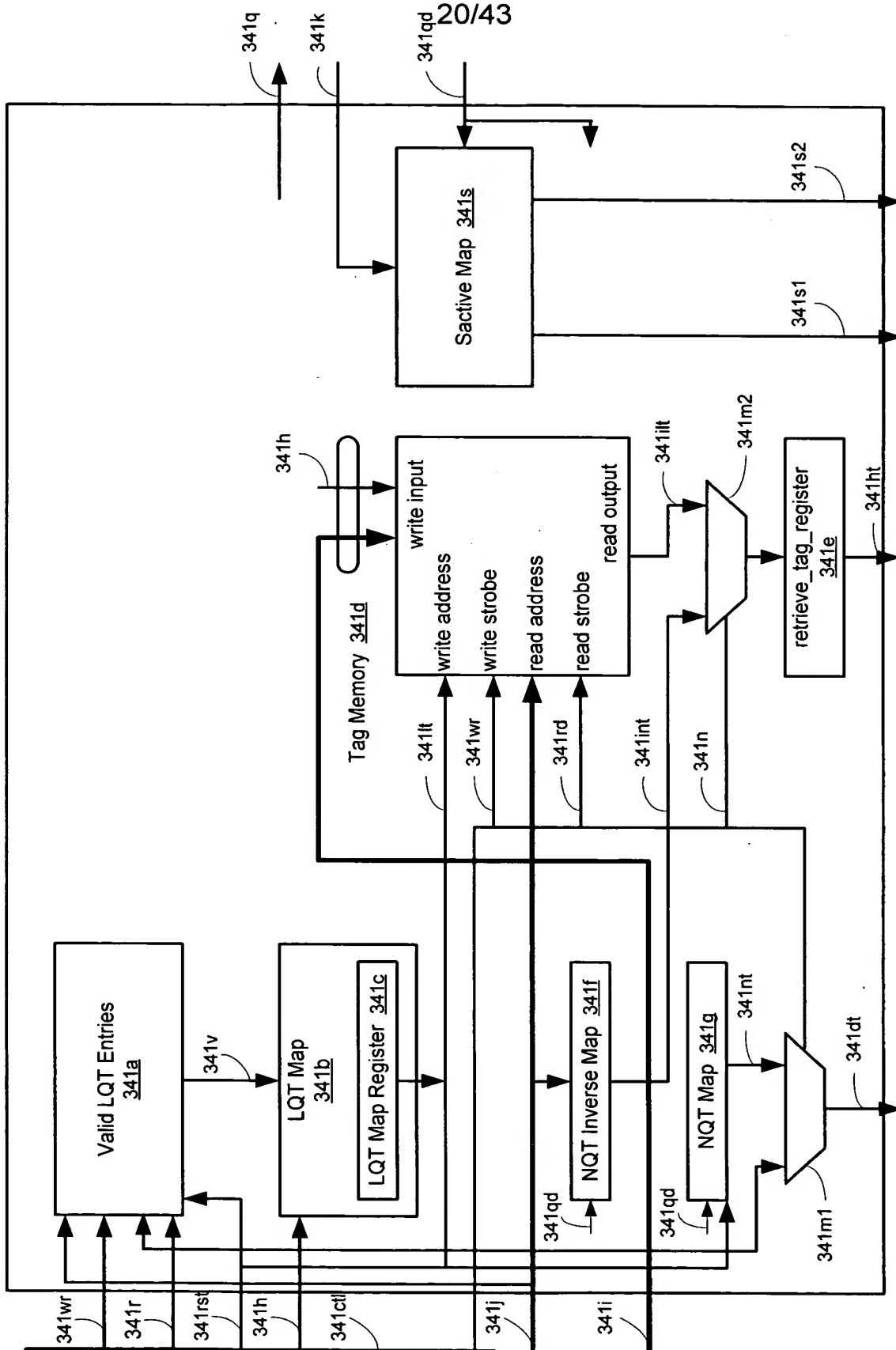


FIG. 7b

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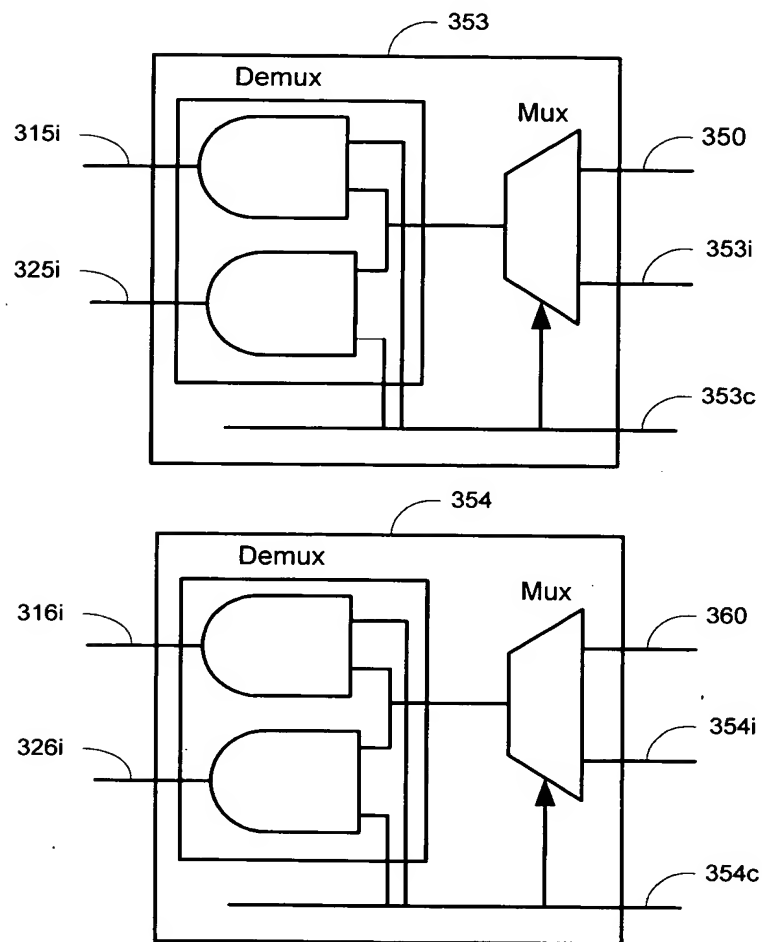
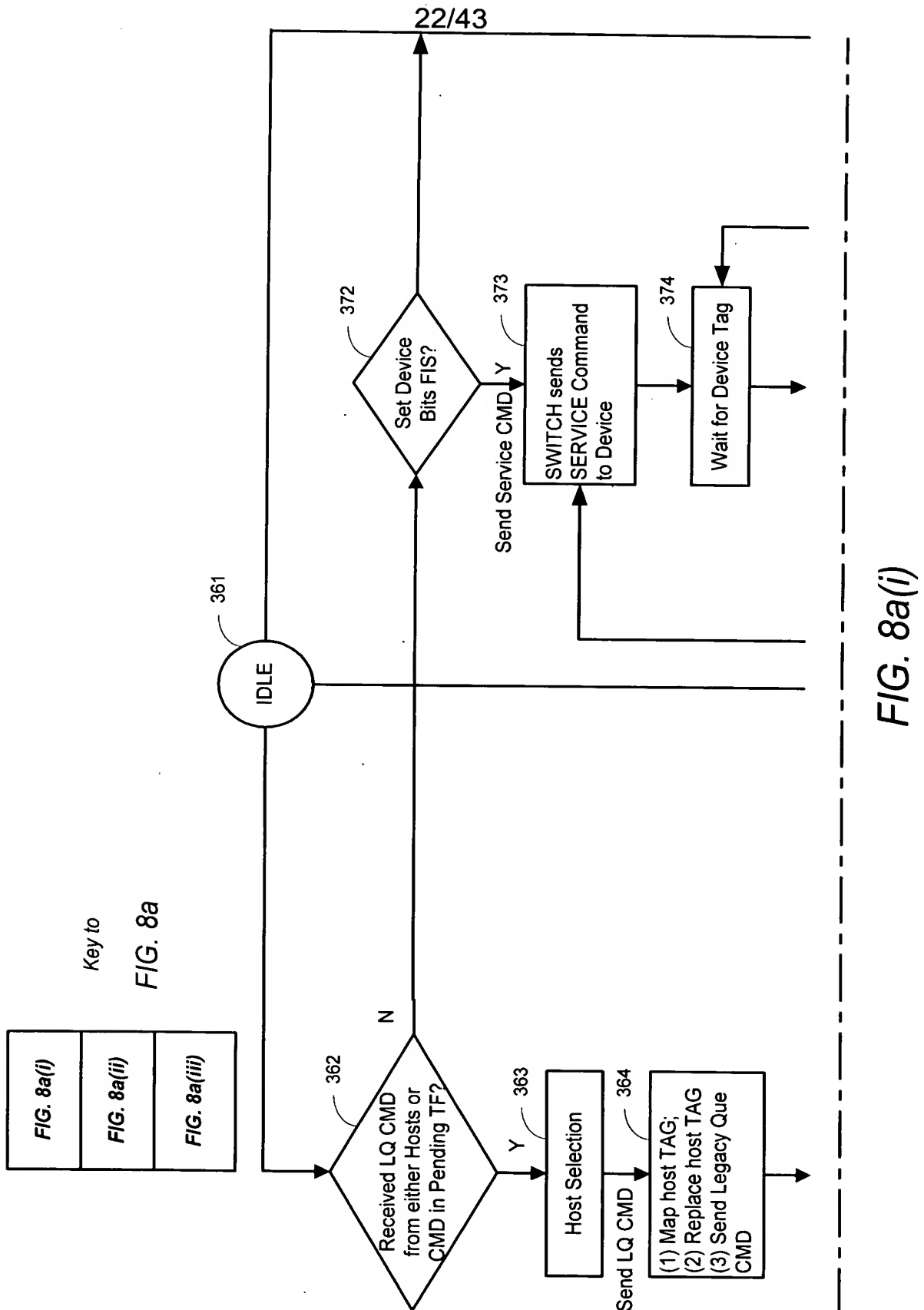


FIG. 7c



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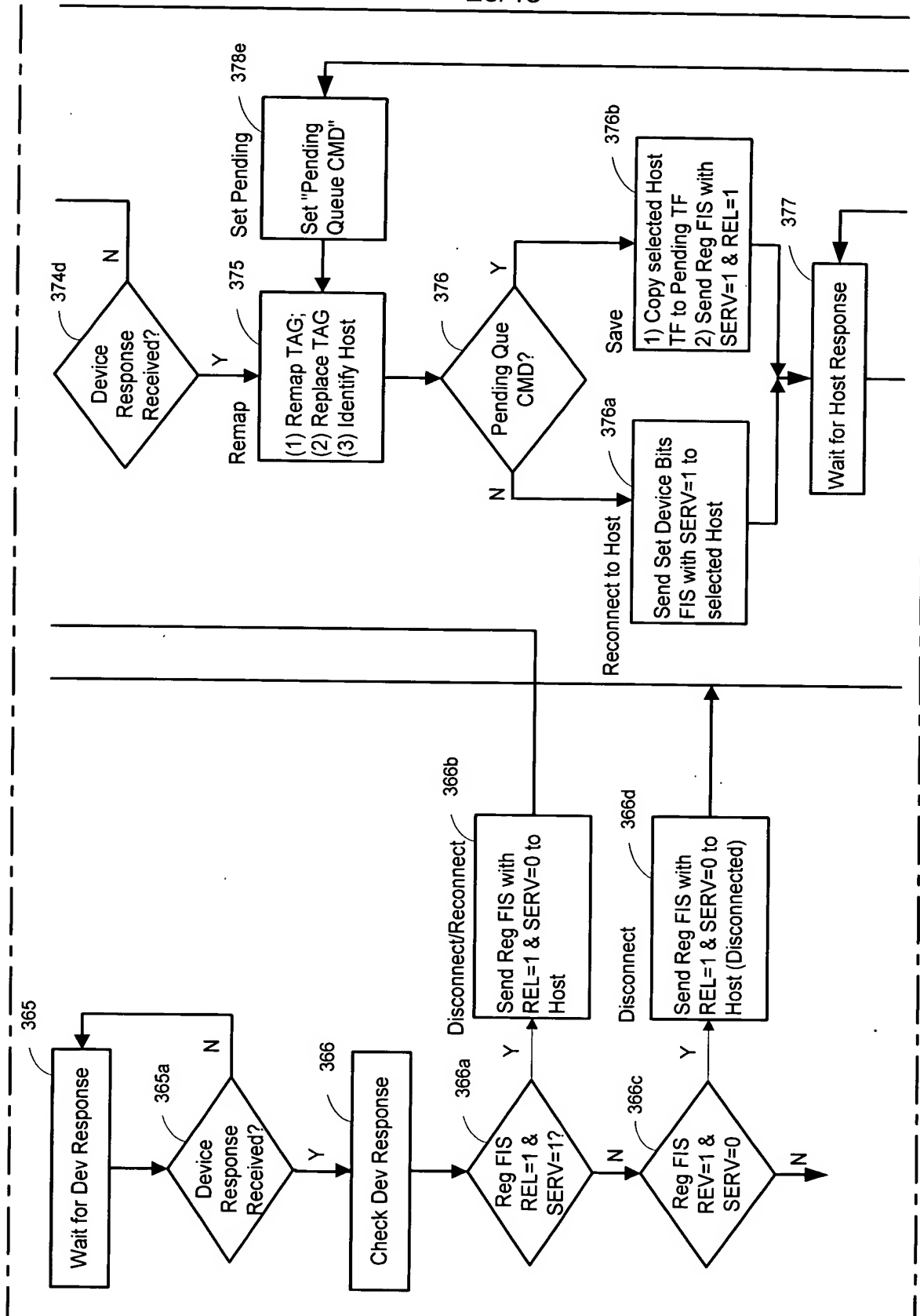


FIG. 8a(ii)

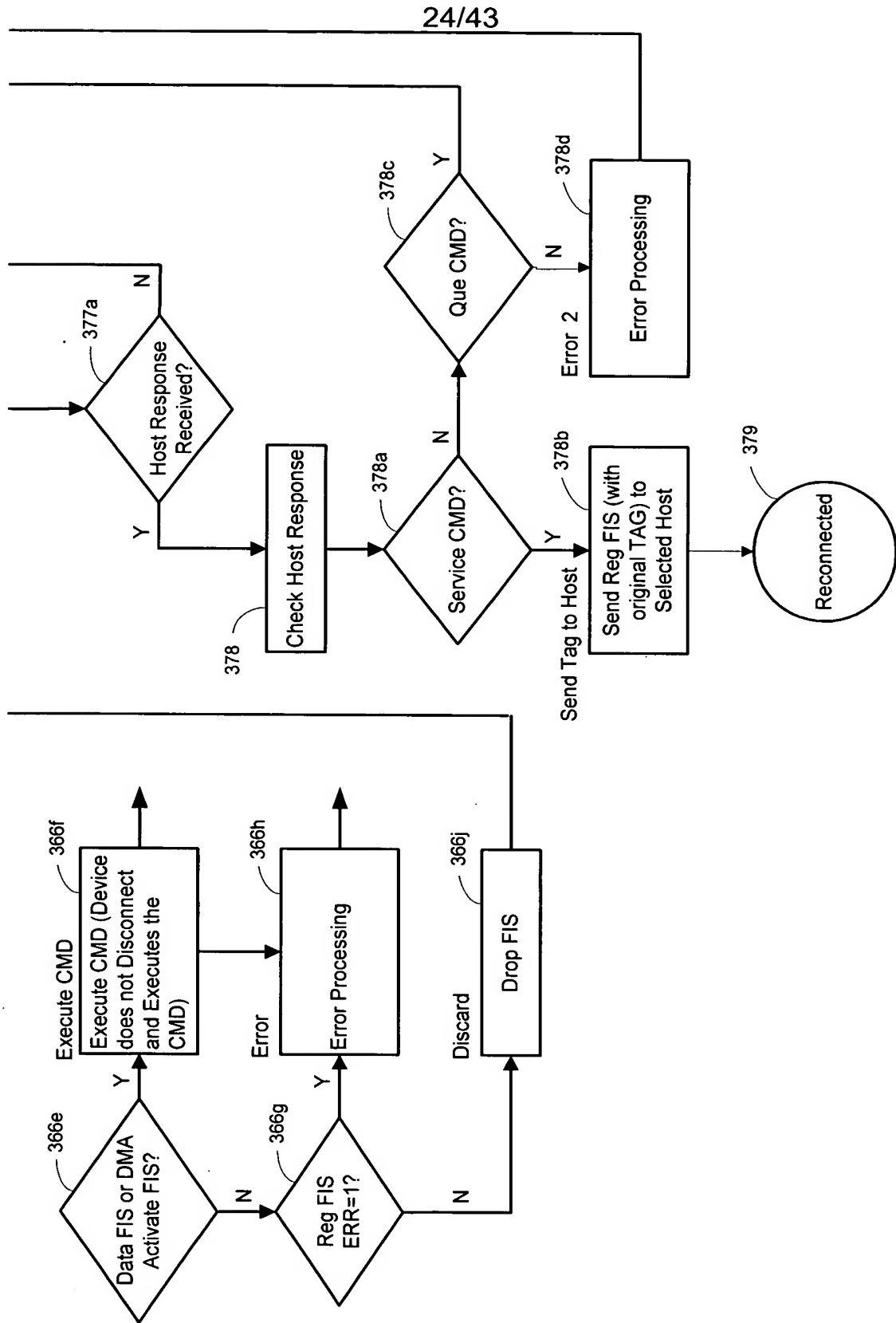


FIG. 8a(iii)

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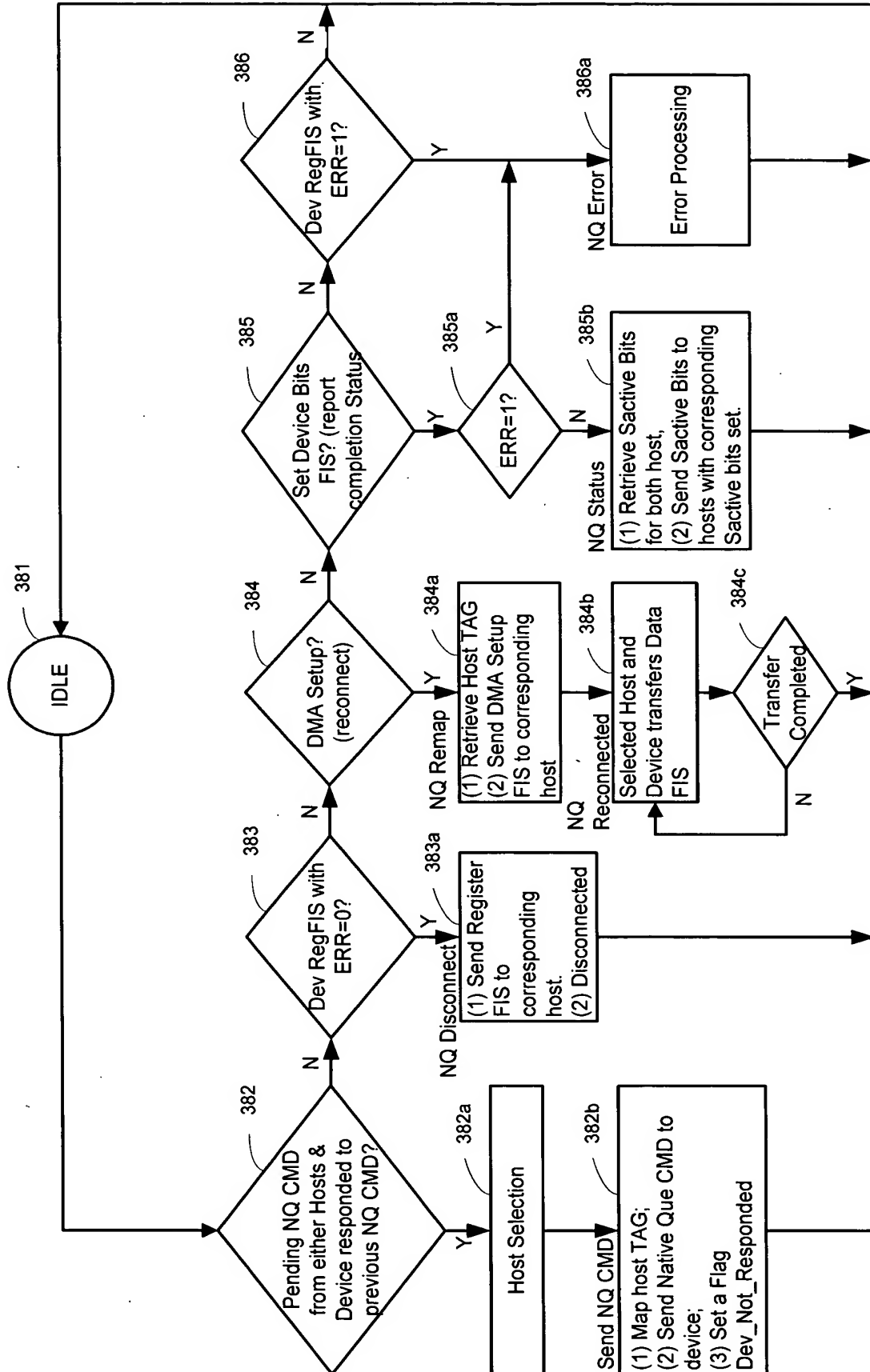


FIG. 8b

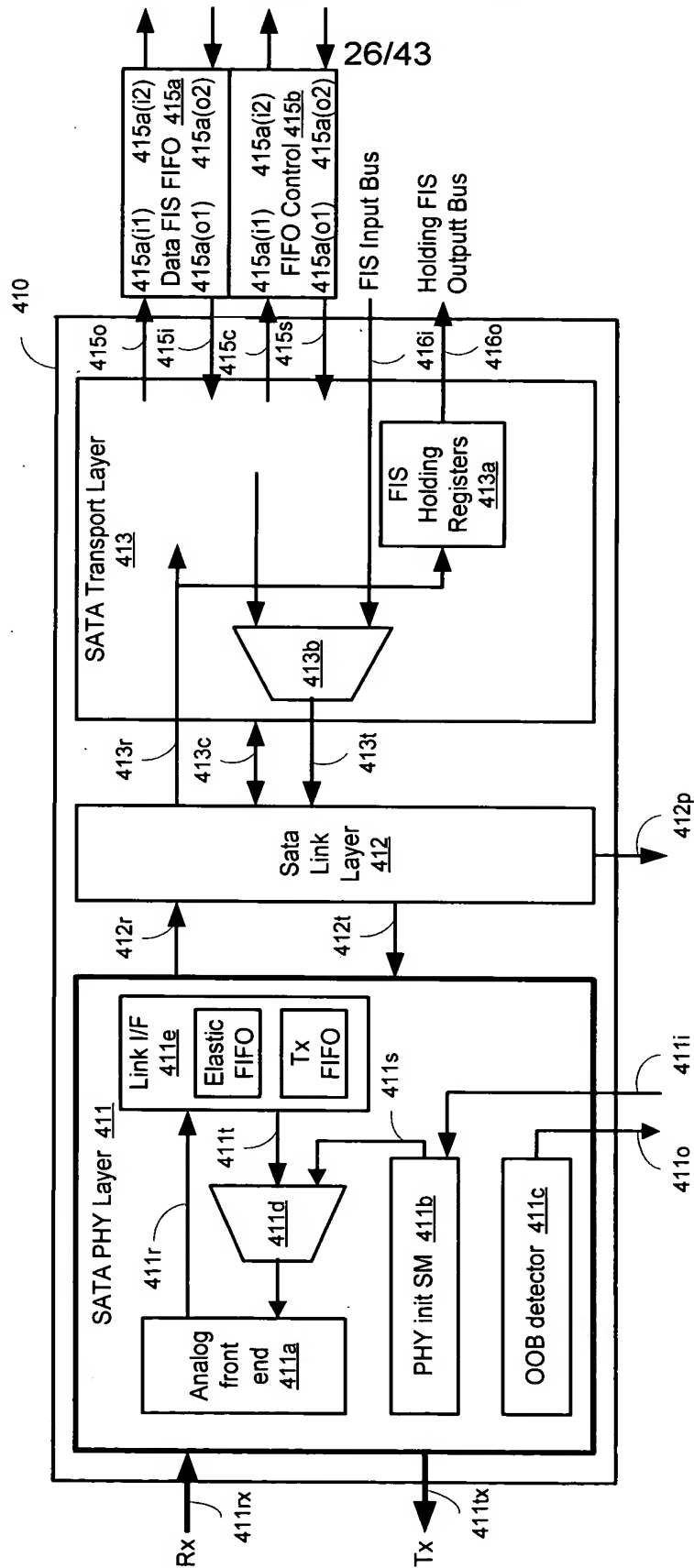


FIG. 9

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FIG. 10a(i)	FIG. 10a(ii)	FIG. 10a(iii)
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Key to

FIG. 10a

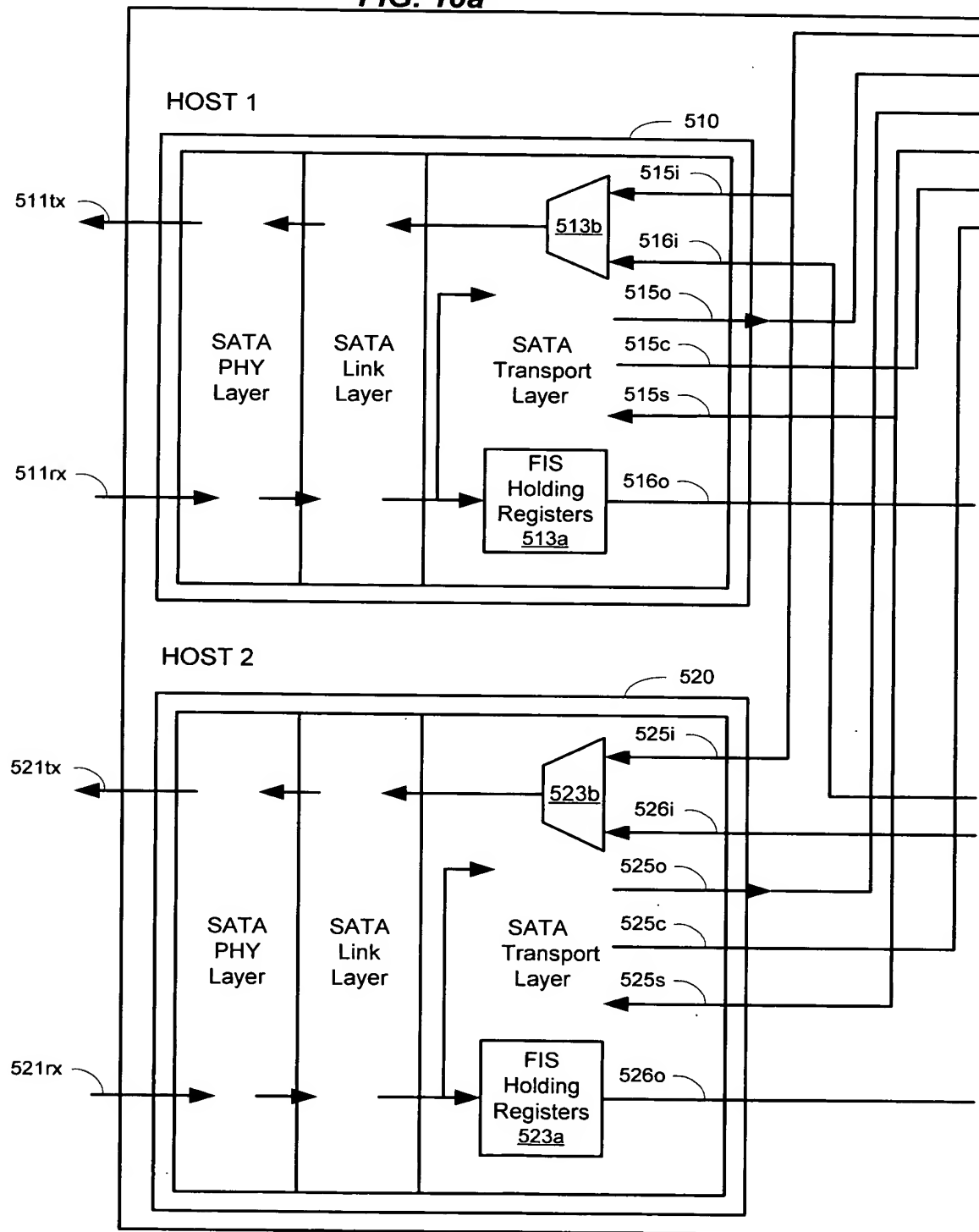


FIG. 10a(i)

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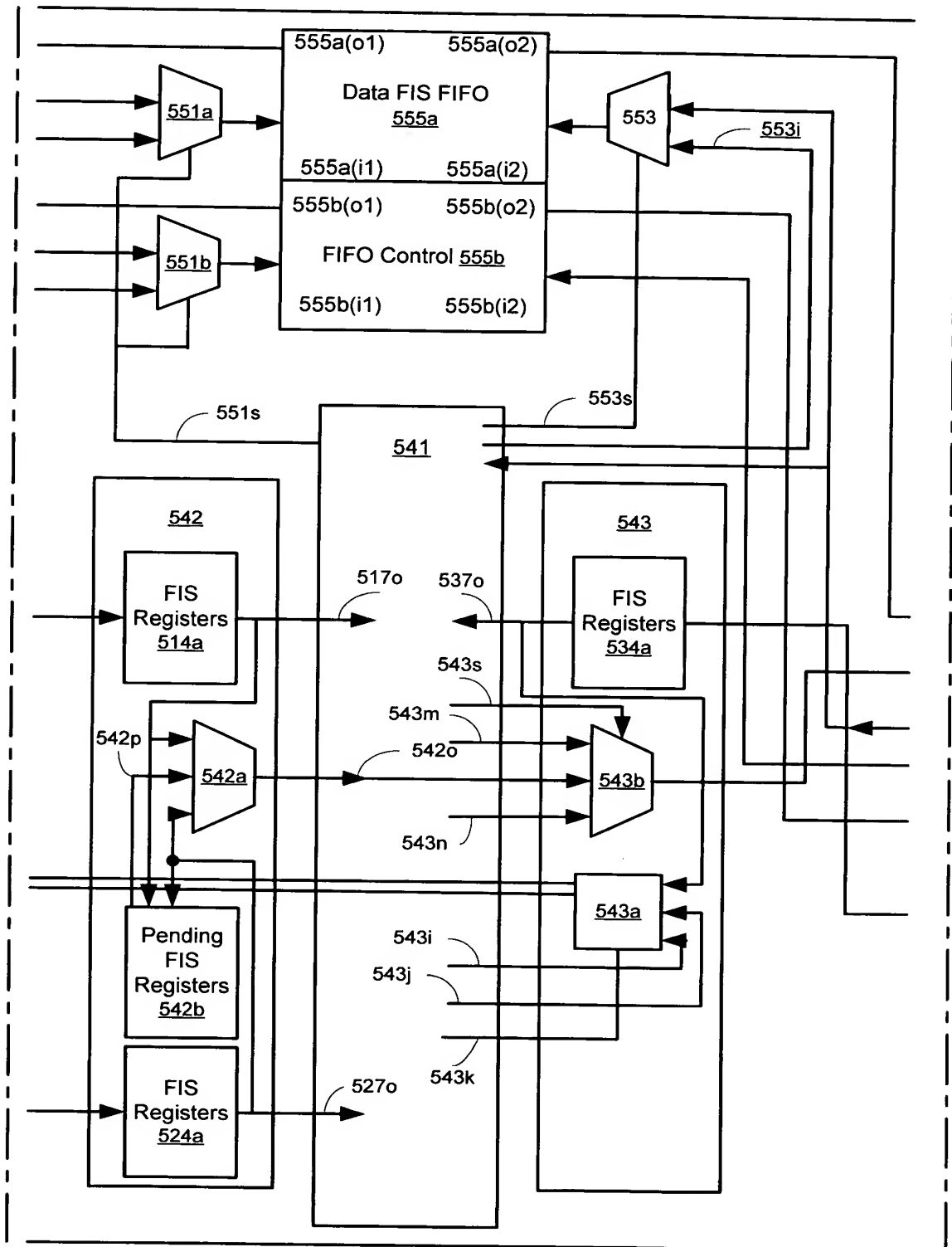


FIG. 10a(ii)

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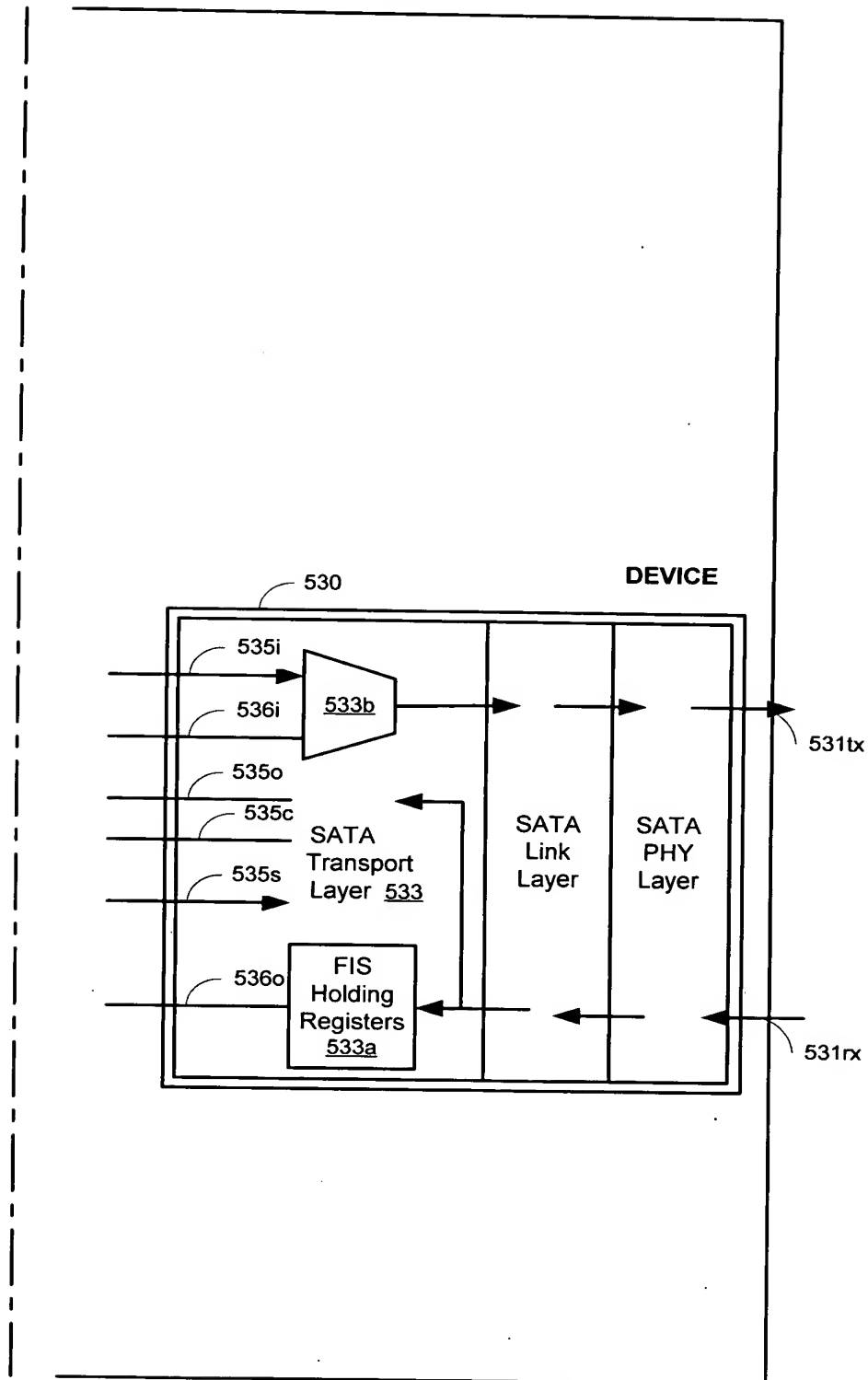


FIG. 10a(iii)

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FIG. 10b(i)

FIG. 10b(ii)

FIG. 10b(iii)

Key to

FIG. 10b

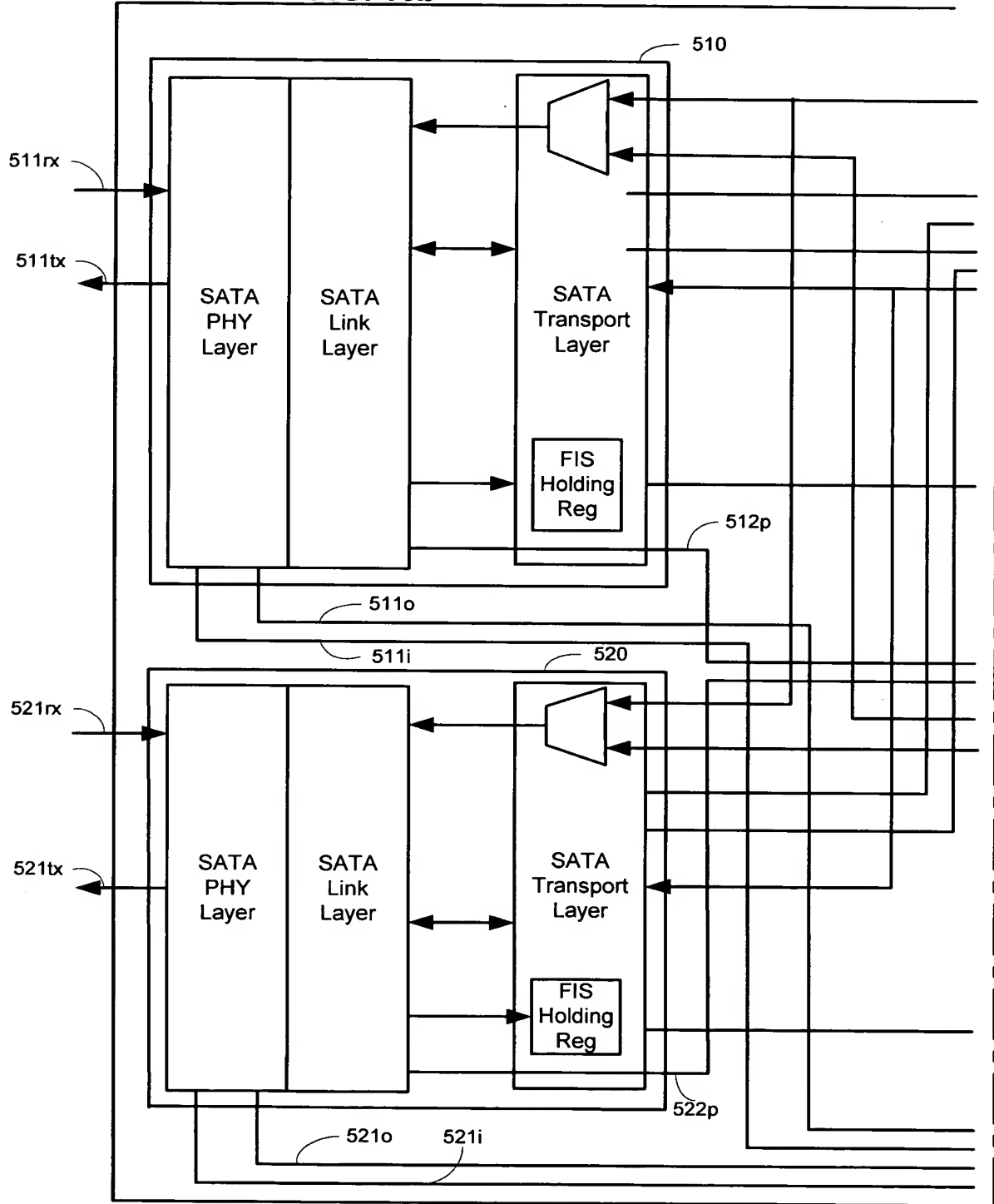


FIG. 10b(i)

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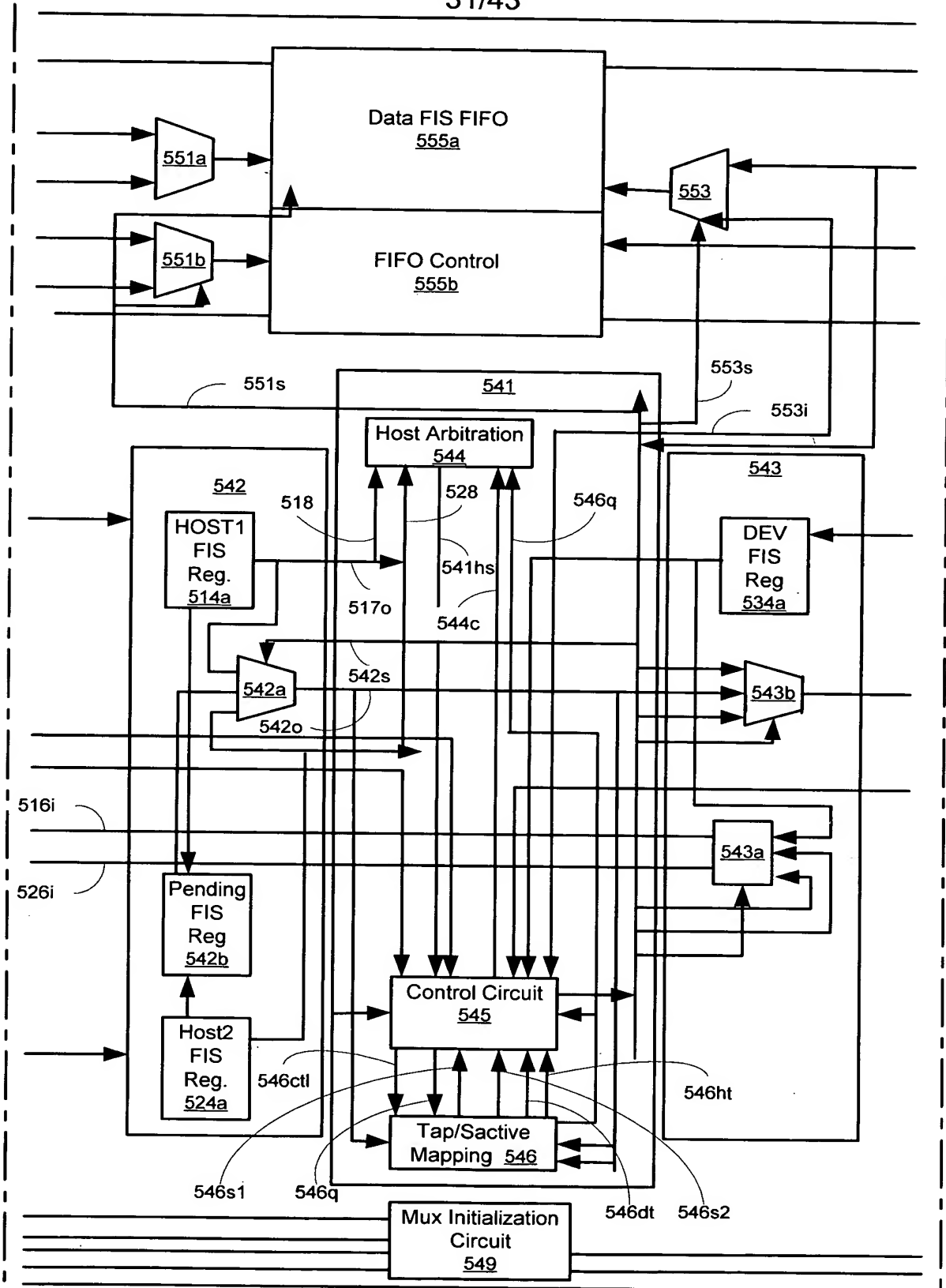


FIG. 10b(ii)

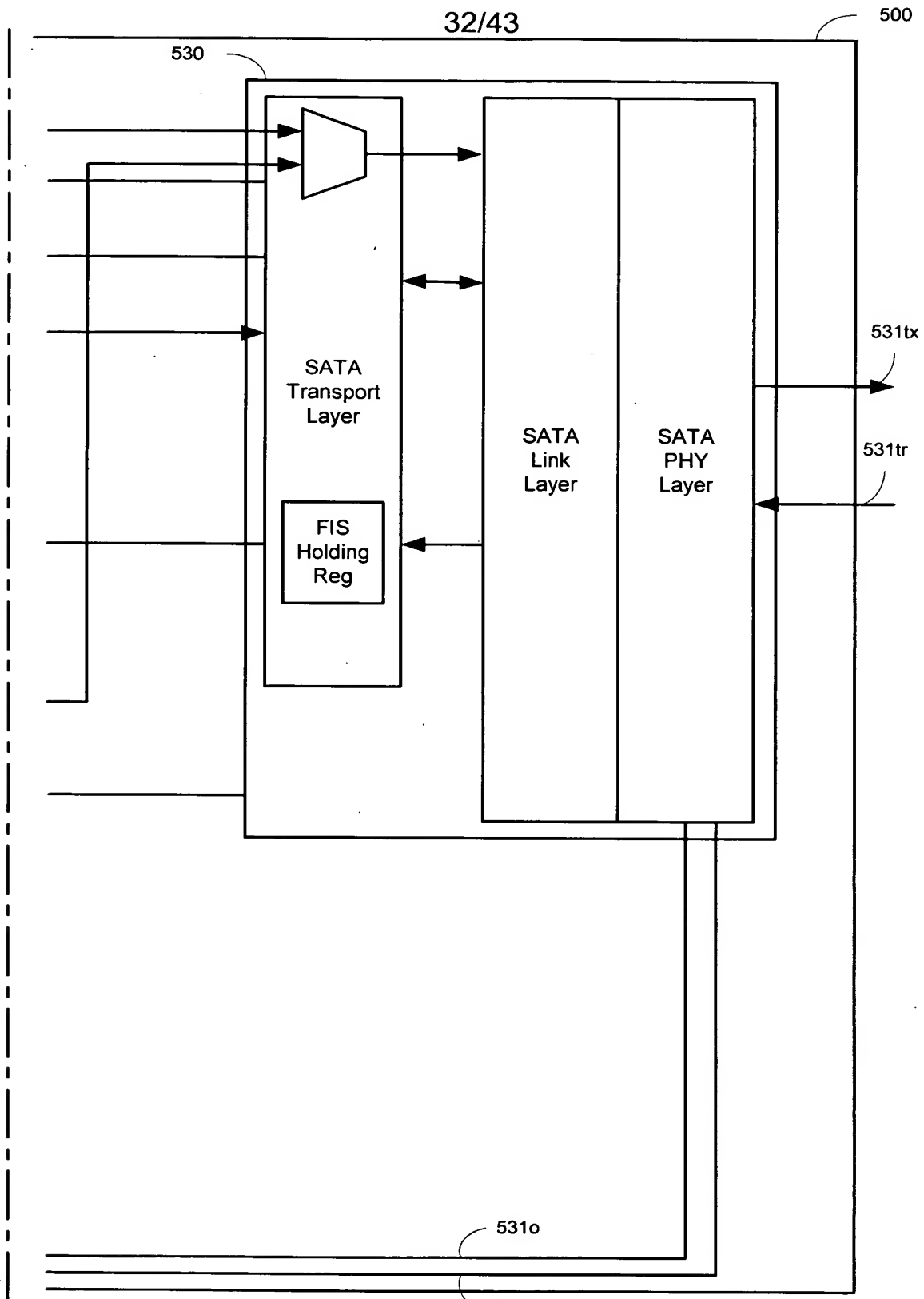


FIG. 10b(iii)

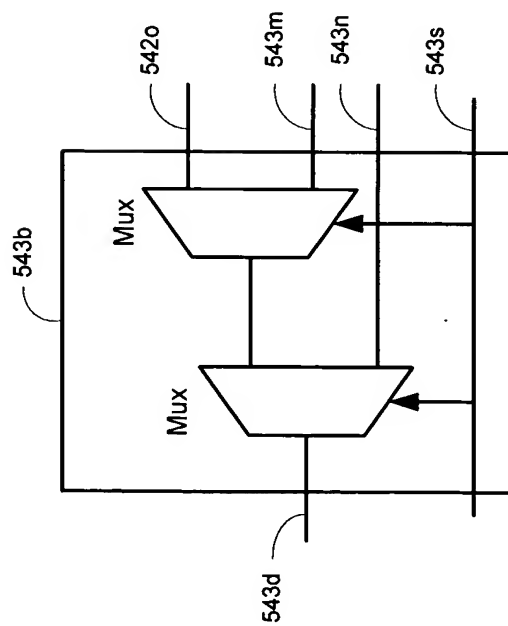
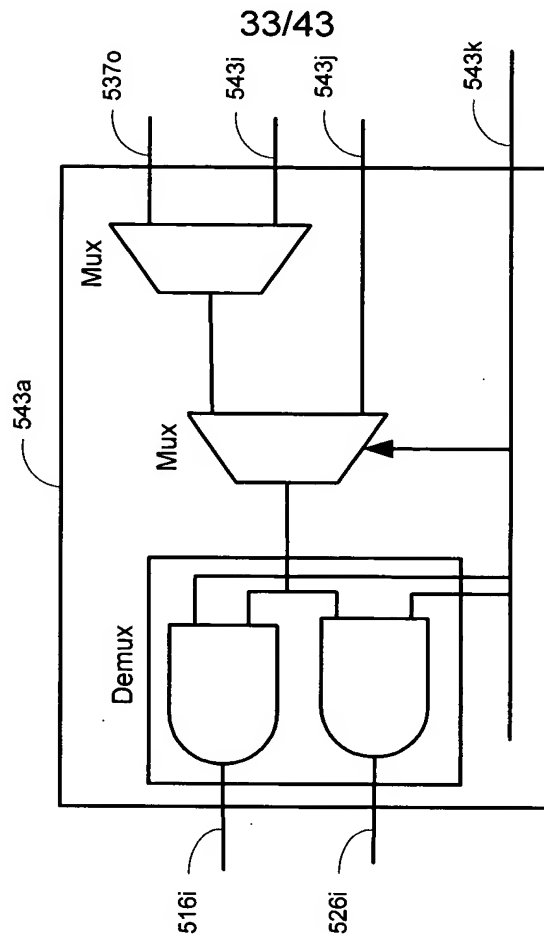


FIG. 10c

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FIG. 11a(i) FIG. 11a(ii)

Key To

FIG. 11a

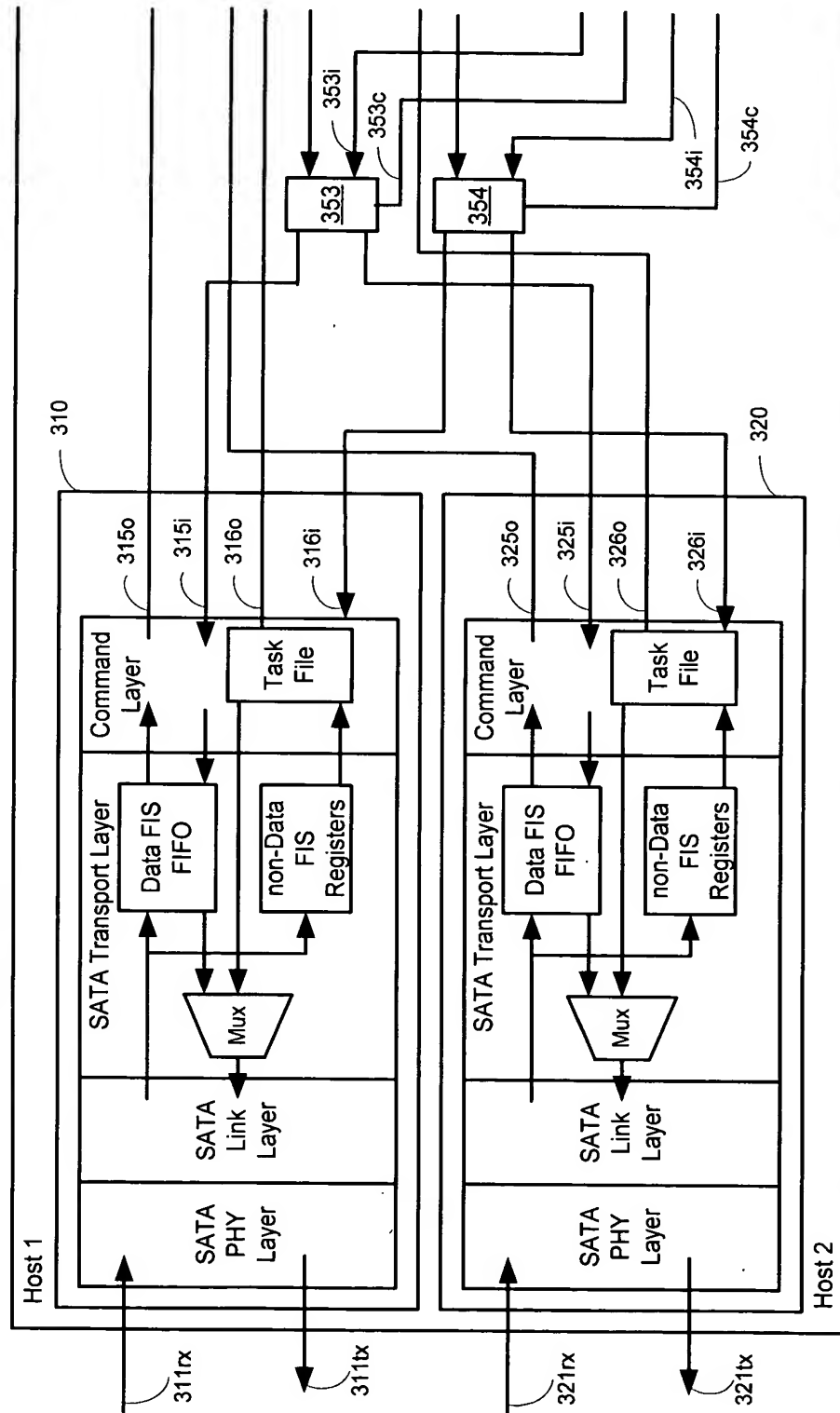


FIG. 11a(i)

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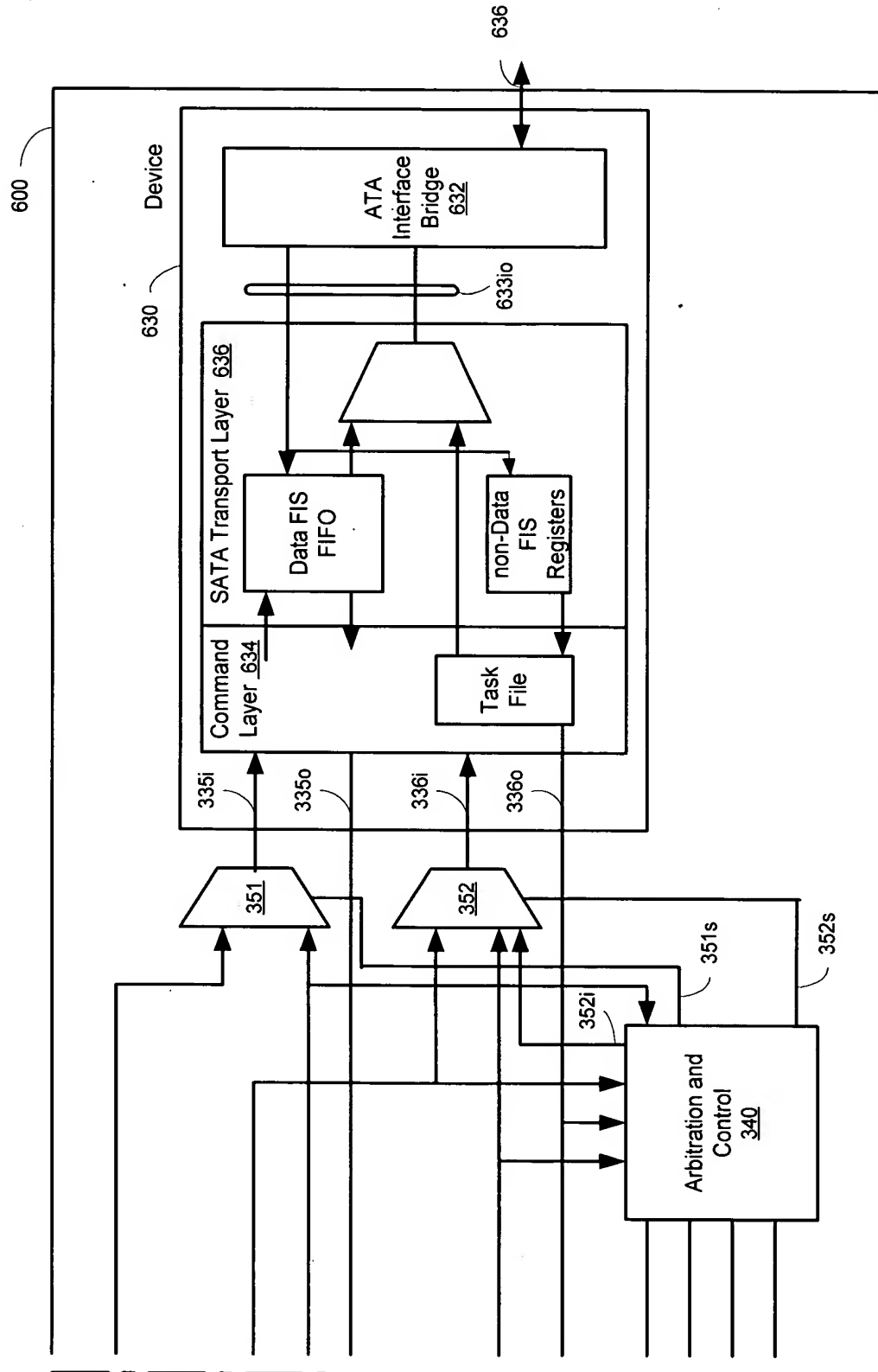
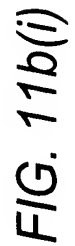


FIG. 11a(ii)



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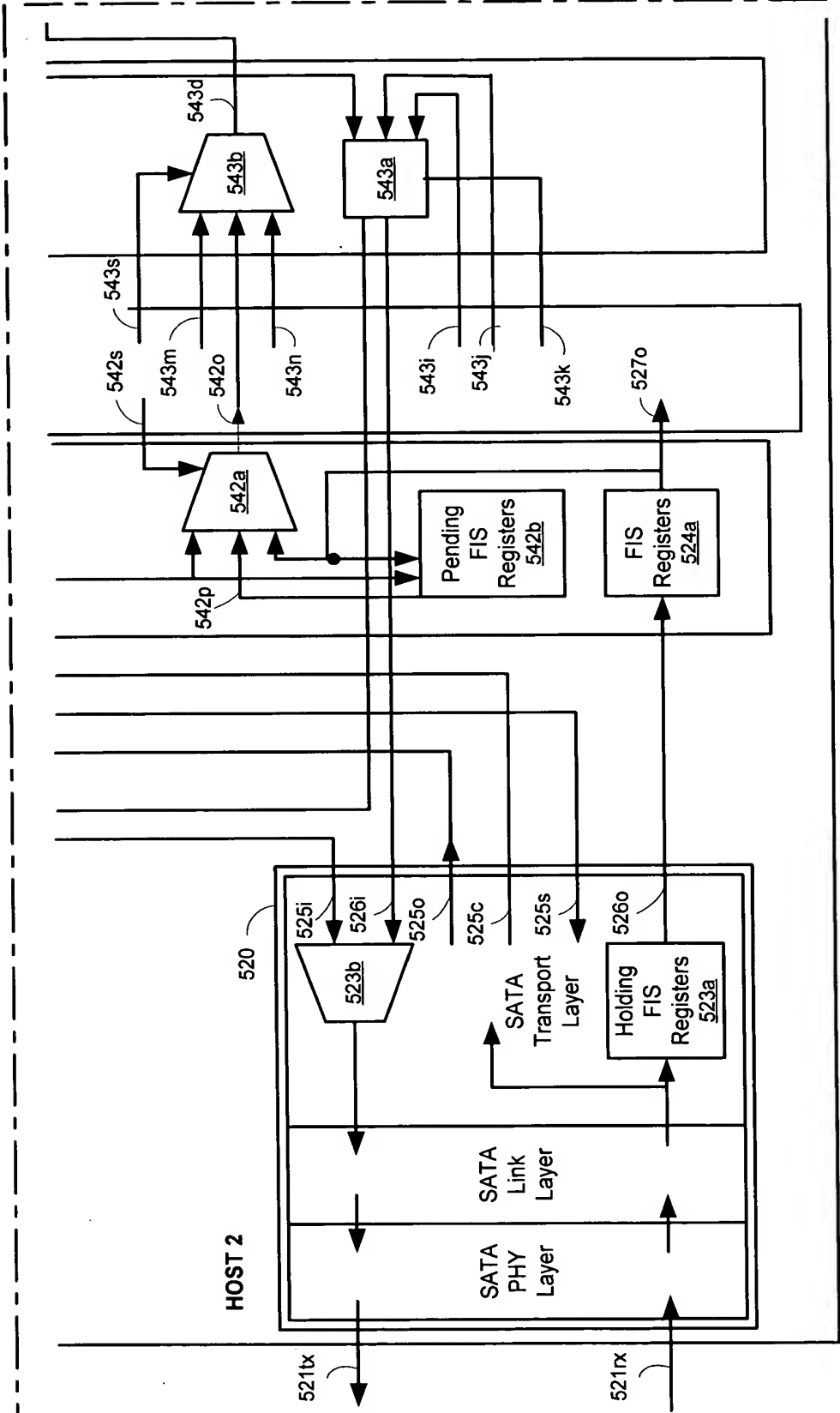


FIG. 11b(ii)

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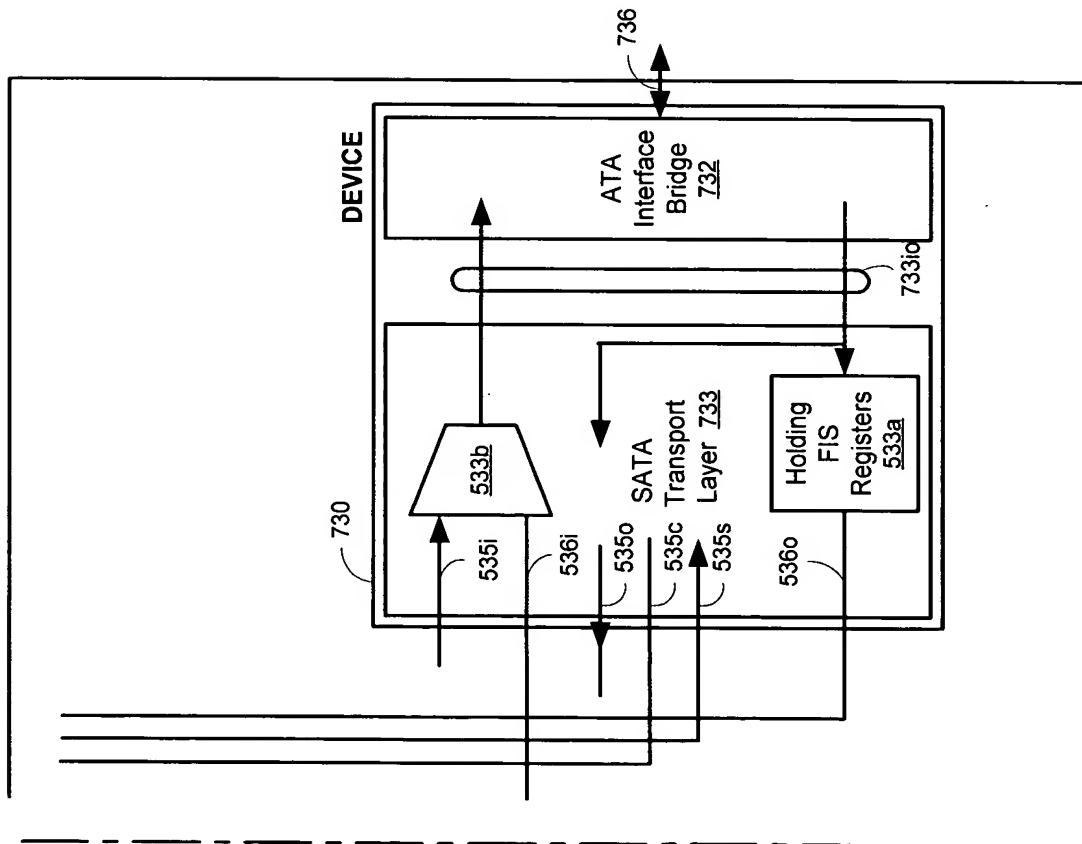


FIG. 11b(iii)

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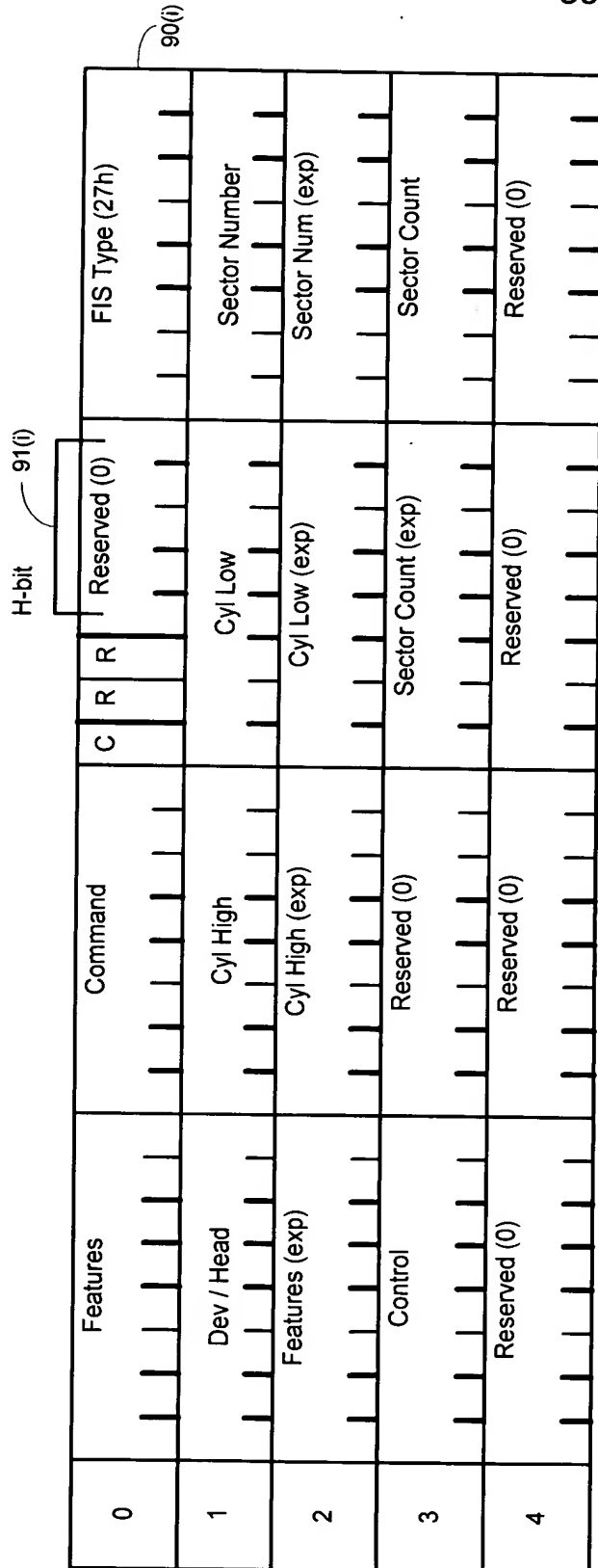


FIG. 12(i) Register FIS Host to Device

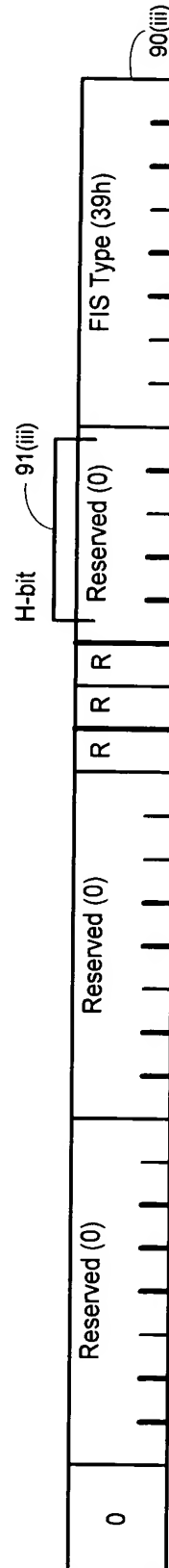


FIG. 12(iii) DMA Activate FIS, Device to Host

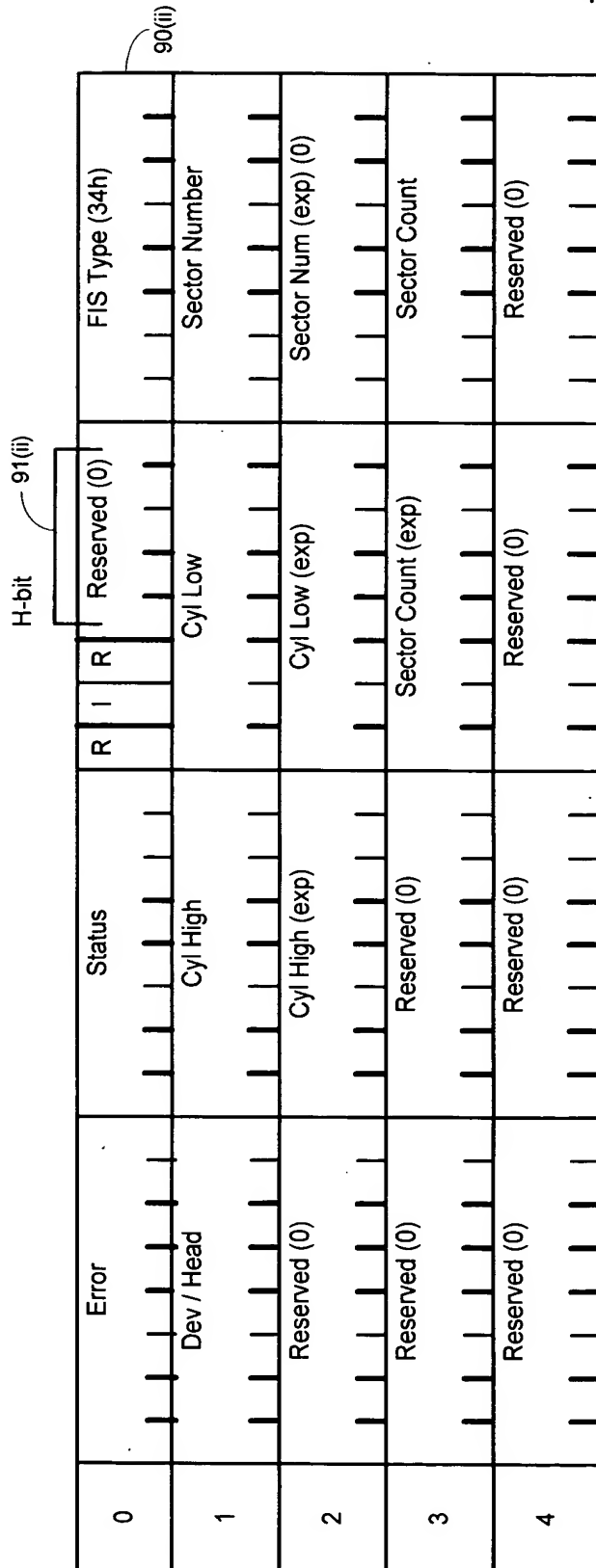


FIG. 12(ii) Register F/S Device to Host

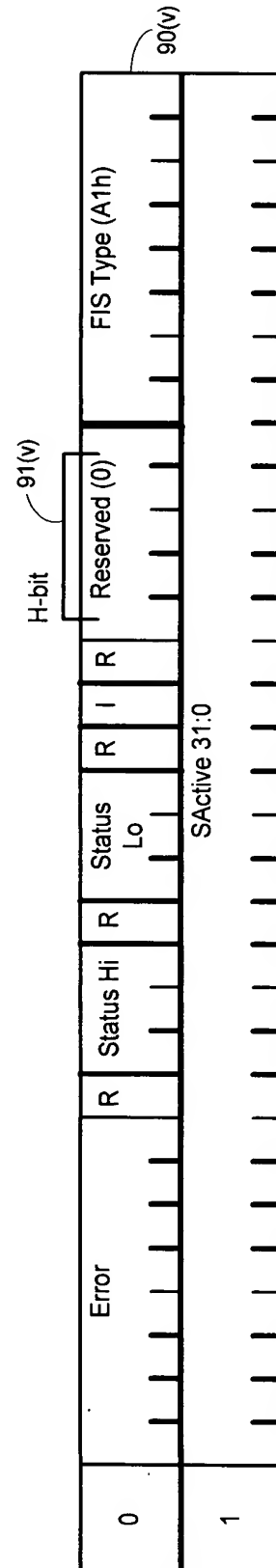


FIG. 12(v) Set Device Bits FIS

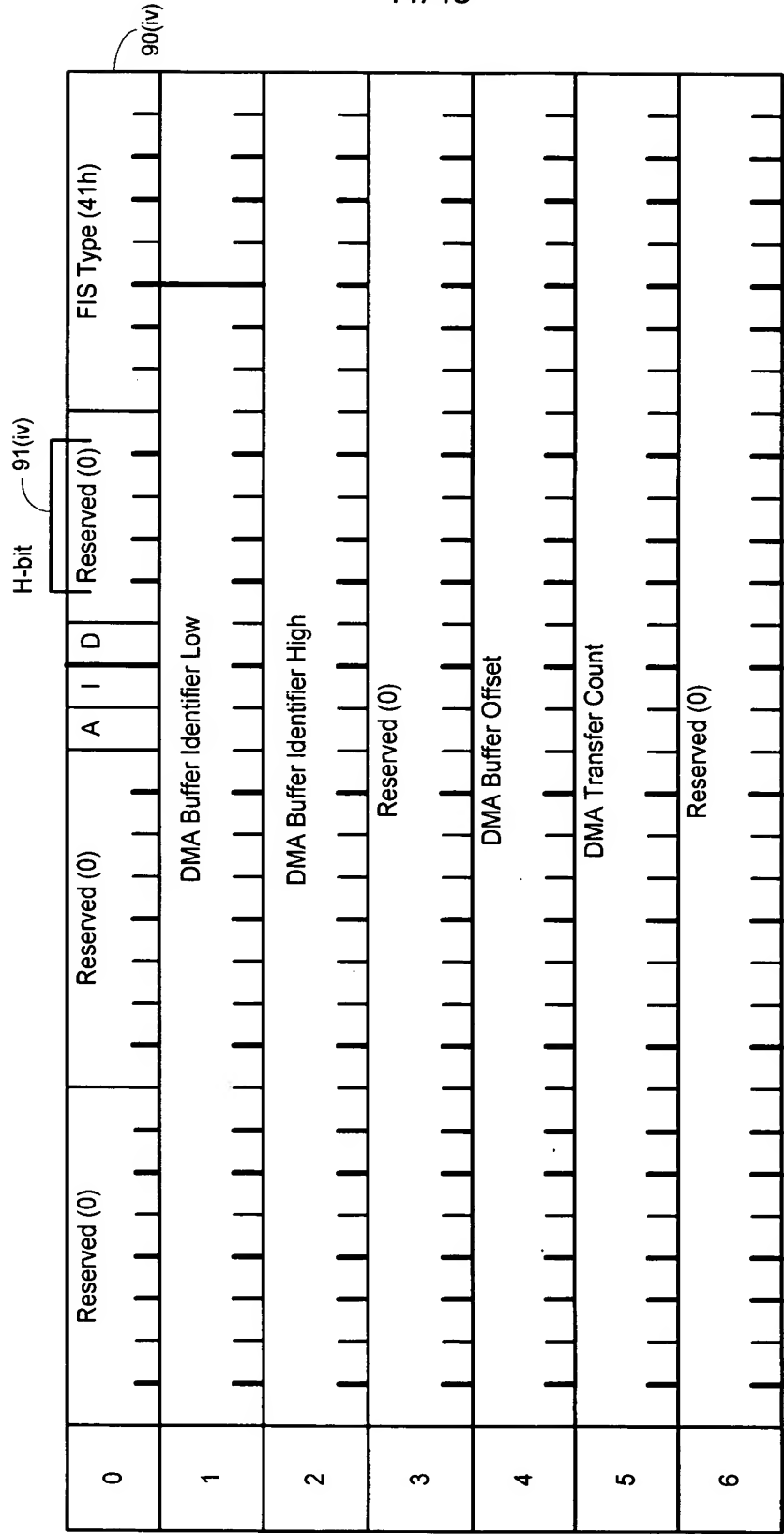


FIG. 12(iv) DMA Setup FIS

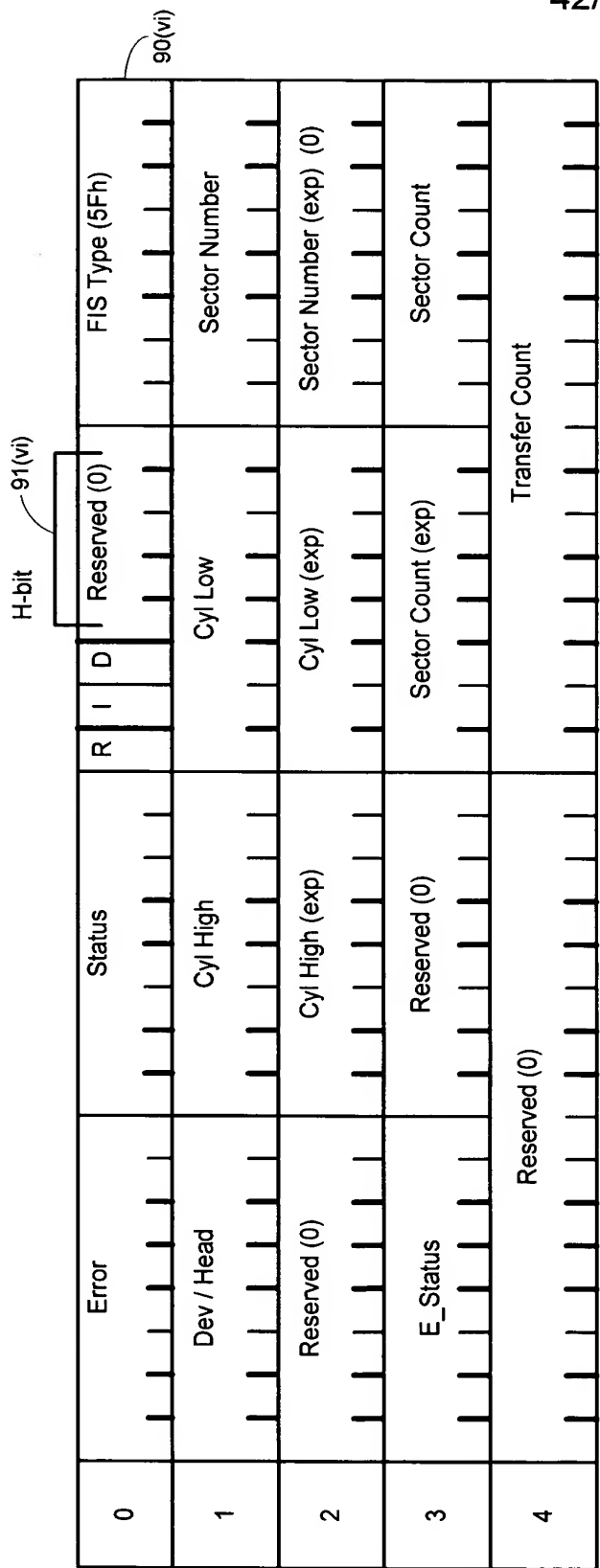


FIG. 12(vi) PIO Setup FIS

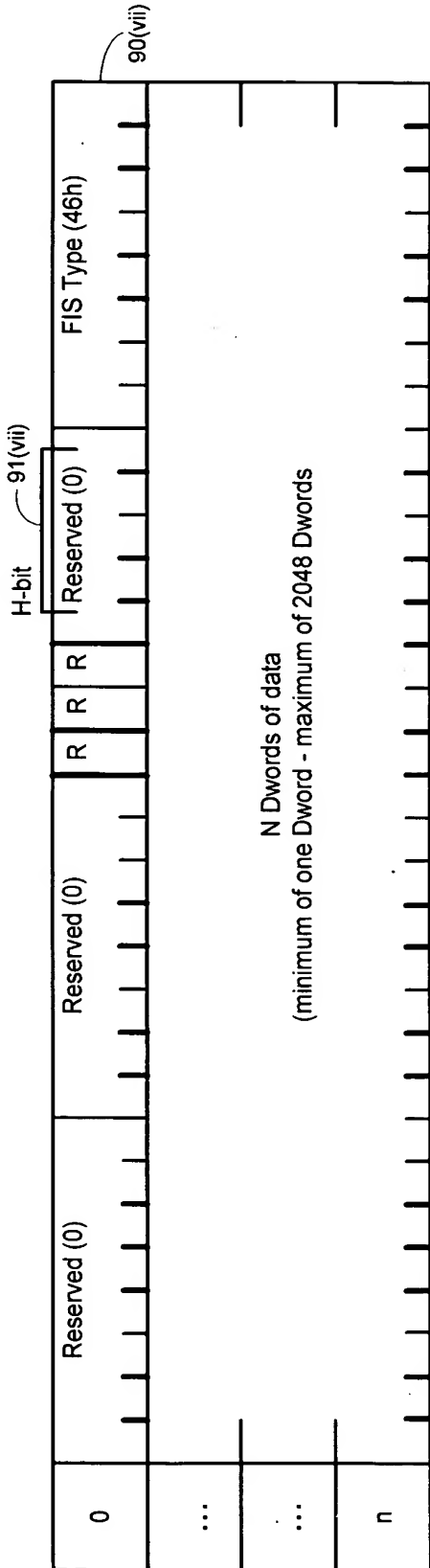


FIG. 12(vii) Data FIS

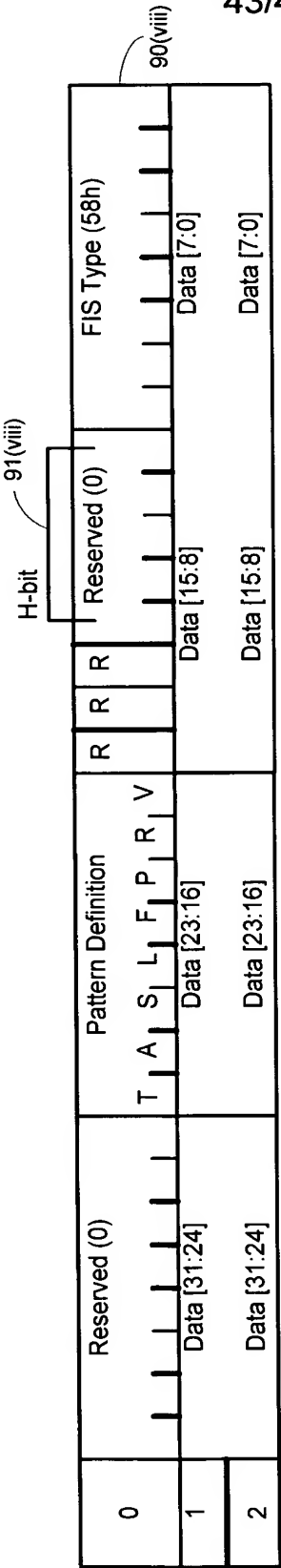


FIG. 12(viii) BIST Activate FIS